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SYSTRON DONNER
Member THORN EMI Group

MODEL 604XA
FREQUENCY COUNTER

INSTRUMENT DIVISION

OPERATING AND SERVICE MANUAL

2727 Systron Drive • Concord, California 94518 • U.S.A.
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January 1982

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CHAPTER 1
GENERAL INFORMATION

1.1 DESCRIPTION

The Systron-Donner 604XA Series Programmable Counters are designed for application where straight forward measurement of communication frequencies are required. The 604XA Series was designed to be compatible with the IEEE-488 interface standard. All front panel controls are programmable except the POWER switch.

A group of LED's on the front panel indicate the status of the instrument while actively in the system. With a quick glance, the operator can determine the address, whether the instrument is in remote or whether a talk only mode has been selected.

The display provides not only the frequency measured but also shows whether the instrument is gating or is in an overflow condition.

The B INPUT channel is protected against overloads with a front panel replaceable fuse. If the input is overloaded, the fuse will open, protecting the B INPUT Amplifier A1 from damage. To replace the fuse simply remove the fuse holder (part of the BNC connector) and insert a new fuse. This eliminates the need to remove the instrument from the rack and disassemble it.

All of these features are contained in only 1-3/4 inches of rack space. This makes the 604XA Series the ideal solution for requirements where space is a factor.

1.2 SPECIFICATIONS

Table 1-1 lists the specifications applicable to the 604XA Series Counters.

TABLE 1-1 SPECIFICATIONS

FREQUENCY MEASUREMENT		
Range:		
	A INPUT (6041A, 6042A, 6043A)	20 Hz to 100 MHz.
	B INPUT (6042A)	100 MHz to 512 MHz.
	B INPUT (6043A)	100 MHz to 1.25 GHz.
Sensitivity:	A INPUT	25 mV rms 20 Hz to 1 MHz. 50 mV rms 1 MHz to 5 MHz. 100 mV rms 5 MHz to 100 MHz.
	B INPUT	-15 dBm 100 MHz to 1.25 GHz.
Resolution:		0.1 Hz to 1 kHz in five decade steps, Front Panel switch selectable or bus programmable.
Accuracy:		±1 count ±time base accuracy.
Display:		Eight Digit readout, with autopositioned decimal point and leading zero suppression.

TABLE 1-1 SPECIFICATIONS (Cont'd)

INPUT CHARACTERISTICS	
A INPUT	
Input Impedance:	1 MΩ shunted by 45 pF (dynamic).
Attenuation:	X1, X10, or X100 Front Panel switch selectable or bus programmable.
Maximum Input: (without damage)	500V peak (dc plus ac component), 100 Vrms maximum in X1.
Operating:	250 Vrms, 20 Hz to 10 kHz. 50 Vrms, 10 kHz to 1 MHz. 10 Vrms, 1 MHz to 10 MHz. 5 Vrms, 10 MHz to 100 MHz.
Display Readout:	kHz with autopositioned decimal point.
B INPUT	
Input Impedance:	50Ω.
Sensitivity:	-15 dBm.
Maximum Input:	Fuse protected, fuse opens at ≈5V rms.
Gate Time:	4 ms to 40 ms (6042A). 16 ms to 160 ms (6043A).
Display Readout:	MHz with autopositioned decimal point.
STANDARD TIME BASE	
Crystal Frequency:	10 MHz
Aging Rate after Warm-up:	±2 parts in 10^6 per year.
Short Term Aging Rate:	±5 parts in 10^9 rms for 1 sec. average.
Temperature Variation:	±5 parts in 10^6 from 0 to +50°C.
±10% Change in Line Voltage:	±1 part in 10^7.
Long Term Aging Rate:	±3 parts in 10^7 for 30 days.

TABLE 1-1 SPECIFICATIONS (Cont'd)

GENERAL	
Display:	0.3 inch LED, eight digit inline readout, autopositioned decimal point and leading zero suppression. LED indicators denote measurement units in kHz for A INPUT and MHz for B INPUT.
Temperature Range: (Operating)	0°C to +50°C.
Power:	100/115 or 215/240 Vac (±10%), 48-400 Hz.
Dimensions:	1.75" (4.4 cm) H x 16.25" (52.5 cm) W x 13" (33.0 cm) D.
Weight:	10 lbs. (4.5 kg) net. 17 lbs. (7.7 kg) shipping.

1.3 OPTIONS

Table 1-2 contains a list of options and/or accessories available for the 604XA Series Counters.

TABLE 1-2 OPTIONS AND ACCESSORIES

OPTION/ACCESSORY	DESCRIPTION
OPTION 08 TCXO TIME BASE OSCILLATOR	
Crystal Frequency	10 MHz
Aging Rate after Warm-up:	±1 part in 10^6 per year.
Frequency retrace for off periods to approximately 24 hours:	±5 parts in 10^7 within 15 minutes.
Short Term Aging Rate:	±5 parts in 10^8/day average for 3 days.
Temperature Variations:	TCXO ±1 part in 10^6 over 0 to +50°C.
±10% change in line voltage:	±5 parts in 10^8.
Long Term Aging Rate:	±3 parts in 10^7 for 30 days.
OPTION 32	A and B INPUTS relocated to Rear Panel.

TABLE 1-2 OPTIONS AND ACCESSORIES (Cont'd)

OPTION/ACCESSORY	DESCRIPTION
ACCESSORY	PART NUMBER
Tilt Stand:	067014
1 Meter IEEE-488 Cable:	11707601
2 Meter IEEE-488 Cable:	11707602
4 Meter IEEE-488 Cable:	11707604
Coaxial cable, 6 feet, male BNC connector on each end:	A10338
"T" BNC Connector:	J0622
BNC Terminator, 50 ohm:	RF0014
Spare Input Fuses for the rf input, box of 5 each:	057245

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

The Model 604XA Frequency Counter is shipped in operational condition and is ready for use as received. This chapter outlines the procedures for initial inspection and installation of the instrument. Instructions for reshipment are also included should the unit be returned to Systron-Donner Corporation for service or repair.

2.2 RECEIVING INSPECTION

Prior to accepting the counter from the shipper, inspect the condition of the shipping container for any indication of freight damage. Any sign of such damage must be noted by both the shipper and receiver and should be reported to the insurance investigator.

Immediately following removal of the instrument from the shipping carton, inspect for possible physical damage incurred during shipment. Check surfaces for scratches or dents and note condition of controls and connectors. Should any damage be noted, notify your nearest Systron-Donner representative.

2.3 RESHIPMENT

When the instrument is to be repackaged for shipment, use the original packing materials. Your Systron-Donner field office can provide materials similar to those used for the original factory packaging, or repackage the instrument following these general instructions.

General packaging instructions:

1) Attach a tag to the unit indicating the model number, serial number, name and address of the instrument owner, and a summary of the service or repairs required.

2) Wrap the instrument in heavy paper or plastic prior to placing it into the shipping container.

3) Select a strong carton or wooden box to house the instrument.

4) Use an adequate layer of shock-absorbing material on all sides of the instrument and protect the front panel with additional layers of cardboard. Be certain that there is no movement of the unit within the container.

5) Seal the package with strong tape or metal bands.

6) Mark the shipping container "FRAGILE - DELICATE INSTRUMENT" to ensure careful handling.

7) Be certain that all correspondence refers to full instrument nomenclature (model and serial number).

2.4 POWER REQUIREMENTS

The model 604XA Frequency Counter is supplied with a standard three-conductor power cord which when plugged into an appropriate power receptacle, grounds the unit to protect operating personnel from certain electrical hazards. Whenever the power cord is mated to a two-conductor outlet, a cord adapter plug (properly installed) will provide the same protection.

The instrument operates from an ac power source of either 115 or 230 Vac at 48 to 400 Hz and consumes approximately 30 Watts. The instrument is normally factory wired for 115V operation. Taps on the power transformer are provided to accomodate 230V power.

Prior to connecting the instruemnt to any source other than 115 Vac, ensure that the transformer primaries are properly connected as per Table 2-1.

TABLE 2-1 PRIMARY POWER CONNECTIONS

	T1		T2	
	115	230	115	230
LINE	5	5	1	1
JUMPER	2-5	2-3	1-3	2-3
NEUTRAL	1	1	4	4

2.5 SYSTEM INTERFACE IEEE-488 INSTALLATION & INTERFACE CONSIDURATIONS

The Model 604XA Counter can be operatedd from an instrumentation bus which conforms to IEEE-488. To implement the bus a 24-pin metric demensioned connector is installed on the Rear Panel of the Counter. Refer to Chapter 3 of this manual for detailed information on the IEEE-488 interface operation. Table 2-2 provides the pin designations for the Rear Panel IEEE-488 24-pin connector.

TABLE 2-2 IEEE-488 INTERFACE CONNECTOR

PIN NUMBER	IEEE-488 MNEMONIC
1	DIO1
2	DIO2
3	DIO3
4	DIO4
5	EOI (Inactive)
6	DAV
7	NRFD
8	NDAC
9	IFC
10	SRQ (Inactive)
11	ATN
12	GND (Shield)
13	DIO5
14	DIO6
15	DIO7
16	DIO8 (Inactive)
17	REN
18	GND (Return)
19	GND (Return)
20	GND (Return)
21	GND (Return)
22	GND (Return)
23	GND (Return)
24	GND (Return)

CHAPTER 3
OPERATION

3.1 INTRODUCTION

Operation of the instrument is described in this chapter. A functional description of the front and rear panel controls, connectors and indicators is provided. Turn on and various typical measurement operations are also described in step-by-step procedures.

3.2 FRONT PANEL

The controls, connectors and indicators located on the front panel of the instrument are described in Table 3-1. Figure 3-1 shows the location by index number.

TABLE 3-1 FRONT PANEL FUNCTIONS

INDEX	NAME	FUNCTION
1	ADDRESS 1 (LSB) 2 3 4 5 (MSB)	Five LED indicators which denote 5-bit address assigned by the address switches on assembly A3.
2	REMOTE	LED annunciator, illuminates when the Counter is operating under remote control via the IEEE-488 bus.
3	TALK ONLY	LED annunciator, illuminates when the Counter is placed in the TALK ONLY mode by the internal PROG/ TALK ONLY switch.
4	Display	An 8-digit seven-segment LED in-line readout, with autopositioned decimal point and leading zero suppression provides the numerical readout of the measured frequency

TABLE 3-1 FRONT PANEL FUNCTIONS (Cont'd)

INDEX	NAME	FUNCTION
	Display (Cont'd)	in kHz (A INPUT) or MHz (B INPUT).
5	MHz	LED annunciator, illuminates when the B INPUT is selected to indicate that the 8-digit display reading is in MHz.
6	kHz	LED annunciator, illuminates when the A INPUT is selected to indicate that the 8-digit display reading is in kHz.
7	GATE	LED annunciator, on during measurement gate time.
8	O.S.	LED annunciator, illuminates when the display readout exceeds 99999999, thus indicating that the Counter has overscaled and a different RESOLUTION selection is required for proper frequency measurement.
9	POWER	Alternate action pushbutton switch, controls the Counters line power.
10	RESET	Momentary pushbutton switch, manually resets the Counter to zero. When released the Counter will start a new Measurement cycle.

TABLE 3-1 FRONT PANEL FUNCTIONS (Cont'd)

INDEX	NAME	FUNCTION
11	HOLD	Pushbutton switch when pressed and latched the Counter will make a single measurement cycle and display (store) that measurement data indefinitely. To generate a new measurement cycle depress the RESET switch.
12	RESOLUTION Hz 0.1 1 10 100 1000	Five interlocking pushbutton switches. Selects appropriate gate time for 0.1 Hz to 1000 Hz resolution.
13	A INPUT ATTENUATOR X1 X10 X100	Three interlocking pushbutton switches. Selects the A INPUT channel with an attenuation factor of X1, X10 or X100.
14	B INPUT (switch)	Pushbutton switch, when pressed and latched, selects the B INPUT channel as the measurement input.
15	A INPUT (connector)	BNC connector used for inputting signals to the 100 MHz input amplifier.
16	B INPUT (connector) 100 MHz-512 MHz (6042A) 100 MHz-1250 MHz (6043A)	BNC connector used for inputting signals to the prescaler. Fuse protected, opens at ≈5 Vrms overload.

3.3 REAR PANEL

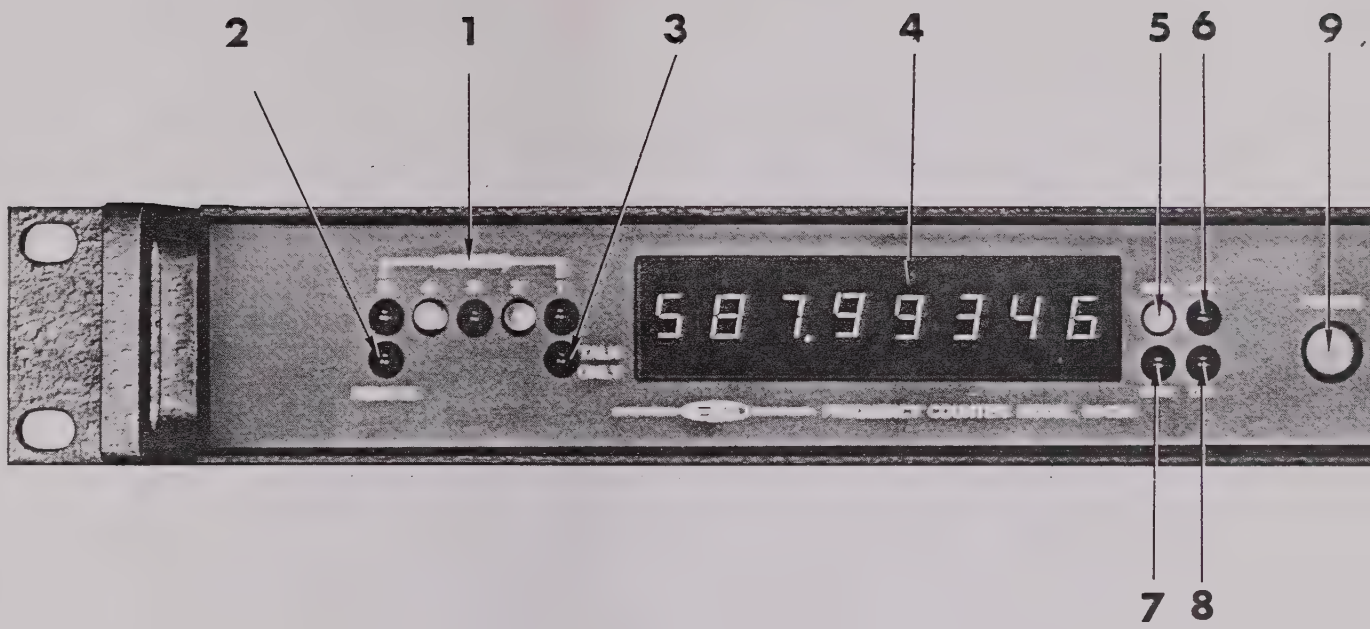
The connectors and controls located on the rear panel of the instrument are described in Table 3-2, and Figure 3-2 shows the location by index number.

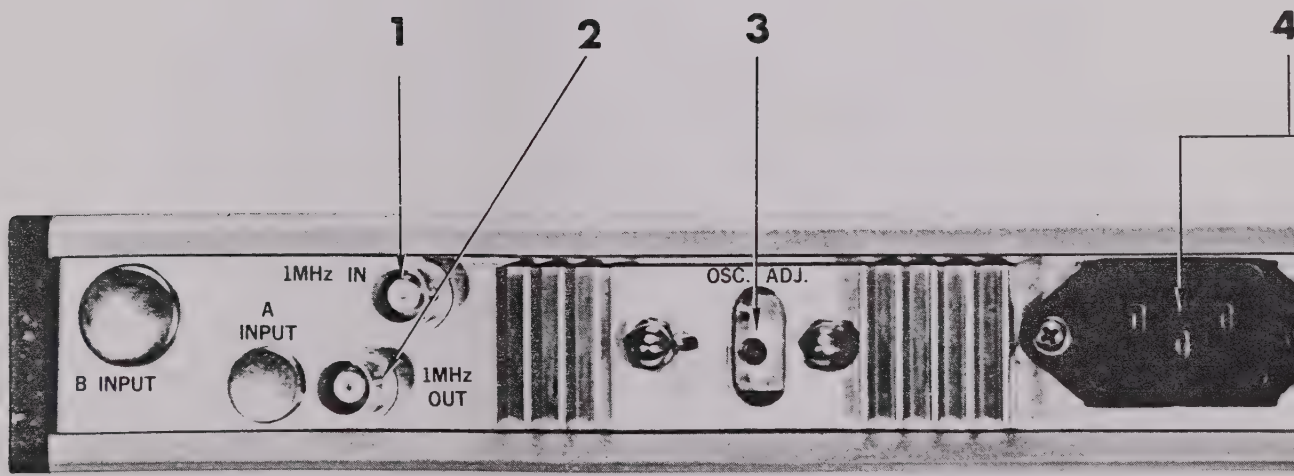
TABLE 3-2 REAR PANEL FUNCTIONS

INDEX	NAME	FUNCTION
1	1 MHz IN	BNC connector, accepts 1 MHz from an external reference for the Counters time base.
2	1 MHz OUT	BNC connector, provides convenience output of the counters internal 1 MHz time base.
3	OSC ADJ	Access slot to oscillator adjustment.
4	Power Connector and Fuse Holder	Power connector and fuse holder .375A or .250A for 115 Vac or 230 Vac respectively.
5	LAMP TEST	Momentary pushbutton switch, when pressed illuminates the 8-digit numerical display providing 88888888 readout, and illuminates the REMOTE indicator.
6	IEEE-488 INTERFACE	A 24-pin IEEE-488 connector to provide instrumentation bus interface. (See Table 3-3)

3.4 INTERNAL OPERATING SWITCHES

The following switches are mounted on the IEEE-488 PCB Assembly (A3) to select the Counters address and mode of bus operation.


2
1
3
4
5
6
9
7
8


1
2
3
4
1MHz IN
A
INPUT
B INPUT
1MHz
OUT
OSC. ADJ.

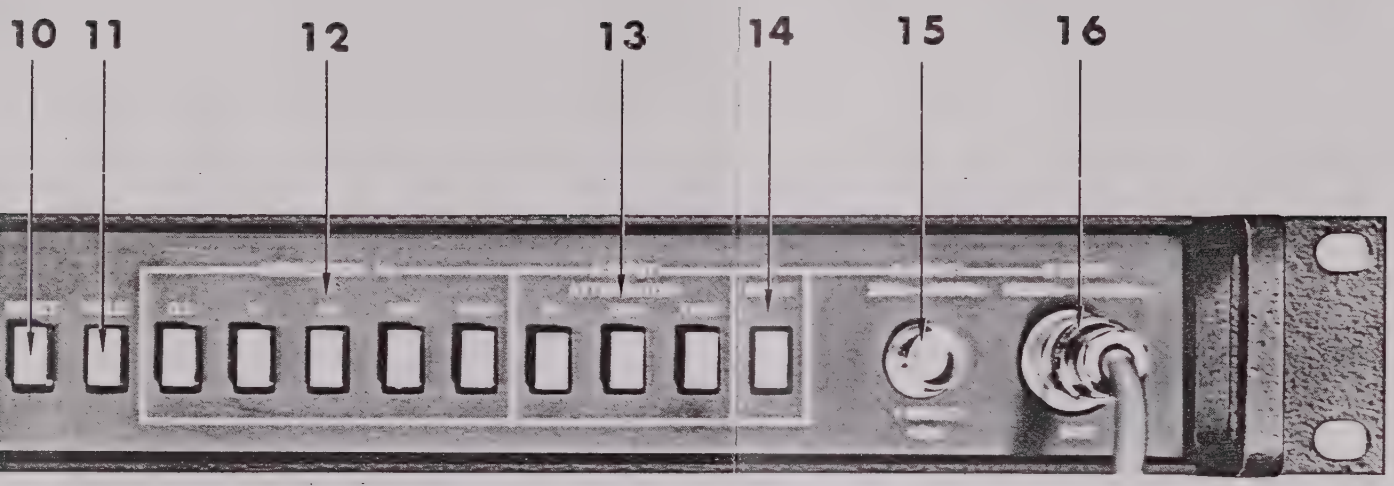


FIGURE 3-1
FRONT PANEL FUNCTIONS

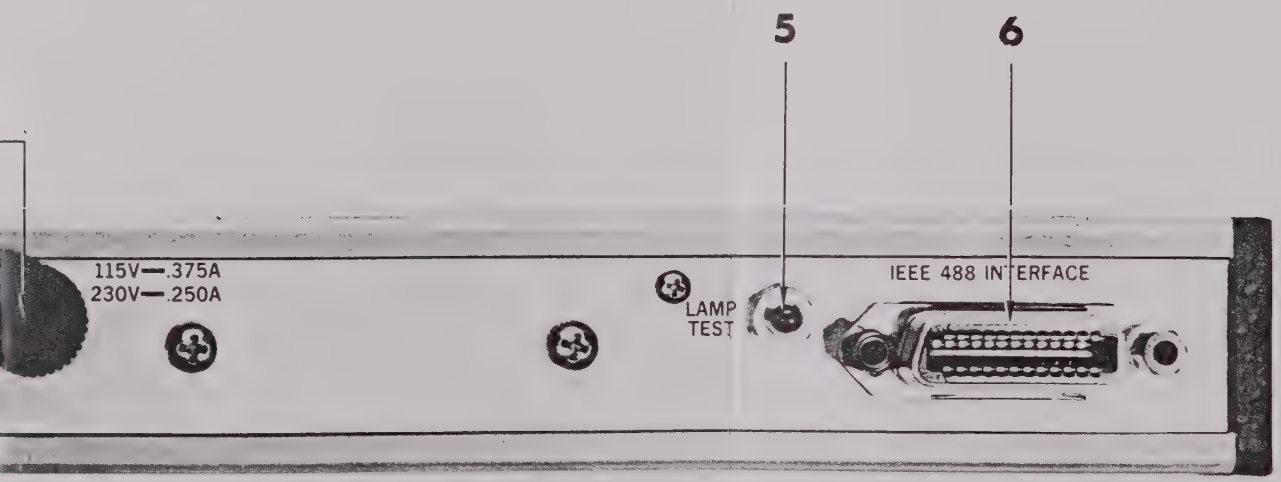


FIGURE 3-2
REAR PANEL FUNCTIONS

3.5.3 IEEE-488 Interface Operational Procedure

The IEEE-488 Interface permits the operation of the Counter from an instrumentation bus. All front panel switch functions other than POWER can be controlled by the bus. The Counter may be used in two different modes of operation, PROGRAMMED or TALK ONLY, as selected by the PROG/TALK ONLY switch located on IEEE-488 Assembly A3.

The Counter may be used on-line or off-line (Remote or Local). The Counter may be programmed as to function, by sending device dependent commands during the Counters "Listen" mode of operation. Device dependent commands are received by the Counter at any time during its operation. The Counter will ignore any command for which it has not been designed or programmed to respond to. When the Counter is addressed to "Talk" data is transmitted in a 15-byte output message, to those devices that are addressed to "Listen".

3.5.3.1 IEEE-488 Subsets Implimented

The following is a list of the interface functions implemented in the 604XA Series Frequency Counters.

SH1	Source Handshake, Full
AH1	Acceptor Handshake, Full
T7	Talk, Basic Talker, Unaddressed if MLA, TON function
TE0	Extended Talker, None
L4	Listen, Basic Listener, Unaddressed if MTA
LE0	Extended Listener, None
SR0	Service Request, None
RL2	Remote Local, No LLO
PP0	Parallel Poll, None
DC0	Device Clear, None
DT1	Device Trigger, Full
C0	Controller, None

NOTE

For complete details on the interface characteristics refer to IEEE-488.

The bus interface lines are assigned IEEE-488 mnemonics which are defined as follows:

DI01 Through DI08: Data Input/Output lines 1 through 8, transmitted message bytes in bit-parallel, byte-serial format, asynchronously and in a bi-directional manner.

DAV: Data Valid, indicates the availability of data on the DI0 lines.

NRFD: Not Ready For Data, indicates when the device is ready to accept data.

ATN: Attention, indicates how the data on the DI0 lines is to be interpreted.

IFC: Interface Clear, is used to set the interface system, and the devices connected to it into a known quiescent state.

NDAC: Data Not Accepted, indicates when the data received was accepted.

SRQ:* Service Request, is used to request service from a controller.

REN: Remote Enable, is used by a controller device (in conjunction with other messages generated in the local logic) to place the Frequency Counter in the Remote Mode of operation.

EOI:* End Or Identify, is used to indicate the end of a data transfer or, with the ATN line to execute a polling sequence.

*These lines are not used by the Model 604XA Counters, and are hardwired high on Assembly A3 - putting a logic 0 on the bus.

Table 3-3 provides the pin designation for the Rear Panel IEEE-488 24-pin connector.

TABLE 3-3 IEEE-488 INTERFACE CONNECTOR

PIN NUMBER	IEEE-488 MNEMONIC
1	DIO1
2	DIO2
3	DIO3
4	DIO4
5	EOI (Inactive)
6	DAV
7	NRFD
8	NDAC
9	IFC
10	SRQ (Inactive)
11	ATN
12	GND (Shield)
13	DIO5
14	DIO6
15	DIO7
16	DIO8 (Inactive)
17	REN
18	GND (Return)
19	GND (Return)
20	GND (Return)
21	GND (Return)
22	GND (Return)
23	GND (Return)
24	GND (Return)

3.5.3.2 Address Assignment Procedure

The Talk and Listen addresses are selected by 5-digit ADDRESS switch A3S1. The setting of the 5-digit code determines which Talk address and corresponding Listen address will be assigned to the instrument. Of the 32 Talk/Listen addresses only 31 may be assigned. Refer to Table 3-4 for the address to ASCII code listing.

NOTE

A 1-1-1-1-1 address must not be assigned to any device interfacing the bus; these addresses are reserved for the unlisten ASCII (?) and the untalk ASCII (_) commands.

TABLE 3-4 TALK/LISTEN ADDRESS ASSIGNMENTS vs. ASCII CHARACTER

ADDRESS SWITCH SETTING BITS					ASCII CHARACTER	
5	4	3	2	1	LISTEN	TALK
0	0	0	0	0	SP	@
0	0	0	0	1	!	A
0	0	0	1	0	"	B
0	0	0	1	1	#	C
0	0	1	0	0	$	D
0	0	1	0	1	%	E
0	0	1	1	0	&	F
0	0	1	1	1	'	G
0	1	0	0	0	(	H
0	1	0	0	1	)	I
0	1	0	1	0	*	J
0	1	0	1	1	+	K
0	1	1	0	0	,	L
0	1	1	0	1	-	M
0	1	1	1	0	.	N
0	1	1	1	1	/	O
1	0	0	0	0	0	P
1	0	0	0	1	1	Q
1	0	0	1	0	2	R
1	0	0	1	1	3	S
1	0	1	0	0	4	T
1	0	1	0	1	5	U
1	0	1	1	0	6	V
1	0	1	1	1	7	W
1	1	0	0	0	8	X
1	1	0	0	1	9	Y
1	1	0	1	0	:	Z
1	1	0	1	1	;	[
1	1	1	0	0	<	/
1	1	1	0	1	=	]
1	1	1	1	0	>	^
*1	1	1	1	1	?	—

* See Note

3.5.3.3 IEEE-488 Multiline Interface Messages

The IEEE-488 messages relate to ASCII code. Table 3-5 provides the IEEE-488 DIO 7-bit code to ASCII character relationship.

TABLE 3-5 IEEE-488 DIO CODE TO ASCII CHARACTER

IEEE-488 DIO BIT							ASCII CHARACTER
7	6	5	4	3	2	1	
0	0	0	1	0	1	0	LF
0	1	0	0	0	0	0	SP
0	1	0	0	0	0	1	!
0	1	0	0	0	1	0	"
0	1	0	0	0	1	1	#
0	1	0	0	1	0	0	$
0	1	0	0	1	0	1	%
0	1	0	0	1	1	0	&
0	1	0	0	1	1	1	'
0	1	0	1	0	0	0	(
0	1	0	1	0	0	1	)
0	1	0	1	0	1	0	*
0	1	0	1	0	1	1	+
0	1	0	1	1	0	0	,
0	1	0	1	1	0	1	-
0	1	0	1	1	1	0	.
0	1	0	1	1	1	1	/
0	1	1	0	0	0	0	0
0	1	1	0	0	0	1	1
0	1	1	0	0	1	0	2
0	1	1	0	0	1	1	3
0	1	1	0	1	0	0	4
0	1	1	0	1	0	1	5
0	1	1	0	1	1	0	6
0	1	1	0	1	1	1	7
0	1	1	1	0	0	0	8
0	1	1	1	0	0	1	9
0	1	1	1	0	1	0	:
0	1	1	1	0	1	1	;
0	1	1	1	1	0	0	<
0	1	1	1	1	0	1	=
0	1	1	1	1	1	0	>
0	1	1	1	1	1	1	?
0	0	0	1	1	0	1	CR
1	0	0	0	0	0	0	@
1	0	0	0	0	0	1	A
1	0	0	0	0	1	0	B
1	0	0	0	0	1	1	C
1	0	0	0	1	0	0	D
1	0	0	0	1	0	1	E
1	0	0	0	1	1	0	F
1	0	0	0	1	1	1	G
1	0	0	1	0	0	0	H
1	0	0	1	0	0	1	I
1	0	0	1	0	1	0	J
1	0	0	1	0	1	1	K
1	0	0	1	1	0	0	L

TABLE 3-5 IEEE-488 DIO CODE TO ASCII CHARACTER (Cont'd)

IEEE-488 DIO BIT							ASCII CHARACTER
7	6	5	4	3	2	1	
1	0	0	1	1	0	1	M
1	0	0	1	1	1	0	N
1	0	0	1	1	1	1	O
1	0	1	0	0	0	0	P
1	0	1	0	0	0	1	Q
1	0	1	0	0	1	0	R
1	0	1	0	0	1	1	S
1	0	1	0	1	0	0	T
1	0	1	0	1	0	1	U
1	0	1	0	1	1	0	V
1	0	1	0	1	1	1	W
1	0	1	1	0	0	0	X
1	0	1	1	0	0	1	Y
1	0	1	1	0	1	0	Z
1	0	1	1	0	1	1	[
1	0	1	1	1	0	0	/
1	0	1	1	1	0	1	]
1	0	1	1	1	1	0	^
1	0	1	1	1	1	1	—

3.5.3.4 Programming Process

The Counters addressing process is controlled by the bus ATN line. The counter is addressed to Talk or Listen by the controller issuing its assigned Talk or Listen address while the ATN line is set active. If the Counter was addressed to Talk, and the controller issues a Talk address other than the Counters assigned Talk address the Counter will automatically deselect itself as a talker. If the Counter was addressed to Talk, and the controller issues the Counters Listen address, the Counter will automatically deselect as a Talker. If the controller issues an untalk (UNT) ASCII — command, the Counter will automatically deselect as a talker. If the Counter was addressed to Listen and the controller issues its Talk address, the Counter will automatically deselect itself as a Listener, and be reassigned as a Talker. If the Counter was addressed to Listen, and the unlisten (UNL) ASCII ? command is

TABLE 3-6 MODEL 604XA PROGRAM FORMAT

BYTE	PROGRAM BITS 7	6	5	4	3	2	1	ASCII CHARACTER	FUNCTION
1	1	0	0	0	0	0	0	@	1 kHz RESOLUTION
	1	0	0	0	0	0	1	A	1 kHz RESOLUTION
	1	0	0	0	0	1	0	B	100 Hz RESOLUTION
	1	0	0	0	0	1	1	C	10 Hz RESOLUTION
	1	0	0	0	1	0	0	D	1 Hz RESOLUTION
	1	0	0	0	1	0	1	E	.1 Hz RESOLUTION
	1	0	0	0	1	1	0	F	.1 Hz RESOLUTION
	*1	0	0	0	1	1	1	G	.1 Hz RESOLUTION
2	1	0	0	1	0	0	0	H	A INPUT X1
	*1	0	0	1	0	0	1	I	A INPUT X10
	1	0	0	1	0	1	0	J	A INPUT X100
	1	0	0	1	0	1	1	K	B INPUT
3	*1	0	0	1	1	0	0	L	HOLD
	1	0	0	1	1	0	1	M	RECYCLE
4	1	0	0	1	1	1	0	N	SAMPLE
	1	0	0	1	1	1	1	O	RESET

*Wake-Up State

issued by the controller, the Counter will deselect as a Listener.

When the Counter is turned on its "wake up" state is as follows:

1. Counter is placed in its "Monitor" mode.

2. The RESOLUTION is set to .1 Hz (ASCII G).

3. The A INPUT X10 is selected (ASCII I).

4. The HOLD control function is selected (ASCII L).

Device dependent data can be programmed into the Counter when its placed in the Remote mode and addressed to Listen. The programmed data may be entered in serial bytes, consisting of 7 parallel bits. The data bytes can be entered in any order and need not be sequential. Table 3-6 provides the program format for the 604XA Counter.

NOTES:

1. Groups 1, 2 and 3 are latched - will retain last function selected in each group as long as instrument is in REMOTE.

2. HOLD - Can talk whenever MTA and EOC are true.

3. Recycle - Can talk only after EOC goes high after an MTA true.

4. TALK - Resets Counter RECYCLE ramp (HOLD).

5. REMOTE - (REN + MLA) or a FUNCTION select (ASCII @ through k entry). Resets Counter for approximately 400 ms.

6. TALK ONLY - After each EOC, Counter will be in the HOLD condition until data is readout to the bus.

3.5.3.5 Output Data Sequence

The Model 604XA Counters outputs measurement data when in the "Talk" mode in a 15-byte, 7-bit format. Table 3-7 shows the data output sequence and the equivalent ASCII characters.

TABLE 3-7 OUTPUT DATA FORMAT

BYTE	BIT 7	6	5	4	3	2	1	ASCII CHARACTER	DATA FUNCTION
1	0	1	0	0	0	0	0	SP	NOT OFFSCALE
1	1	0	0	1	1	1	1	O	OFFSCALE
2	0	1	0	0	0	0	0	SP	NOT OFFSCALE
2	1	0	1	0	0	1	1	S	OFFSCALE
3	0	1	1	X	X	X	X	0→9	10^7 MSD
4	0	1	1	X	X	X	X	0→9	10^6
5	0	1	1	X	X	X	X	0→9	10^5
6	0	1	1	X	X	X	X	0→9	10^4
7	0	1	1	X	X	X	X	0→9	10^3
8	0	1	1	X	X	X	X	0→9	10^2
9	0	1	1	X	X	X	X	0→9	10^1
10	0	1	1	X	X	X	X	0→9	10^0 LSD
11	1	0	0	0	1	0	1	E	Exponent Pointer
12	0	1	0	1	0	1	1	+	Exponent Sign
12	0	1	0	1	1	0	1	−	Exponent Sign
13	0	1	1	X	X	X	X	0→3	Exponent Value
14	0	0	0	1	1	0	1	CR	Delimiter
15	0	0	0	1	0	1	0	LF	Delimiter

Note: Reading Expressed in Hz.
Example: OS 1 2 3 4 5 6 7 8 E − 1 C_R L_F
= 1 2 3 4 5 6 7 8 x 10^{-1} Off Scale
Input Freq. = 21.2345678 MHz

CHAPTER 4

PRINCIPLES OF OPERATION

4.1 INTRODUCTION

This chapter describes the principles of operation of the 6041A/6042A/6043A Frequency Counters. First, a functional block level description is presented, keyed to Figure 4-1. The block level description is generalized, covering the functional blocks within the counter and the signal flow between them. Secondly, a circuit level description is presented, keyed to assembly block diagrams (Chapter 4) and assembly schematics (Chapter 7). The circuit description is more detailed and provides information for troubleshooting to the component level.

4.2 FUNCTIONAL BLOCK DIAGRAM

Refer to the functional block diagram, Figure 4-1, for the following discussion. Input signals are connected to the 604XA Series Frequency Counters via front panel BNC connectors. (Counters with option 32 have rear panel connectors.) Table 4-1 defines the frequency range of the A/B INPUTS for the 604XA series.

TABLE 4-1 604XA SERIES FREQUENCY COVERAGE

Model	A INPUT (J2)	B INPUT (J1)
6041A	20 Hz - 100 MHz	Not Used
6042A	20 Hz - 100 MHz	100 MHz - 512 MHz
6043A	20 Hz - 100 MHz	100 MHz - 1.25 GHz

4.2.1 Input Signal Conditioning

A INPUT signals are coupled to an attenuator on Logic Assembly A2. The A INPUT ATTENUATION step is selected at the front panel, or programmed via the IEEE-488 interface.

B INPUT signals are coupled to Prescaler Assembly A1. Model 6042A uses a 512 MHz prescaler (p/n 6729901) that divides the B INPUT signal by a factor of four (÷4). Model 6043A uses a 1.25 GHz prescaler (p/n 6725001) to divide the B INPUT by 16. Prescaler Assembly A1 provides a sensitivity adjustment for the B INPUT channel. B INPUT connector J1 has an integral fuse (J1F1) that protects Assembly A1 from damage.

4.2.2 Counter Logic

Logic Assembly A2 counts the selected input signal (A or B) and outputs count and scan data to Assemblies A3 and A4. Assembly A2 outputs the 8-digit count one digit at a time, scanning from the most significant digit (MSD) to the least significant digit (LSD). Leading zeros are suppressed and off scale displays are denoted by lighting the O.S. indicator on the front panel. The decimal point is automatically positioned as a function of the input (A or B) and resolution selected.

The value of each digit (0-9) is sent to IEEE-488 Interface Assembly A3 in BCD (8421) format. Each digit is sent to Display Assembly A4 in 7-segment format to drive the front panel LEDs.

4.2.3 Timebase

Frequency Counter accuracy is a function of the time base oscillators' accuracy/stability. A 10 MHz TCXO (Temperature Compensated Crystal Oscillator) provides the internal standard from which all other timing is derived. The 10 MHz internal standard is divided by 10 on Assembly A2 and routed out J4 on the rear panel. A 1 MHz external

standard can be connected to the 604XA series Frequency Counter via J3 on the rear panel. If an external standard is used, logic on Assembly A2 disconnects the internal TCXO. A high stability TCXO is available as option 08.

4.2.4 Systems Interface

Front panel pushbuttons provide the control inputs to Assembly A2 in the local mode. Programming inputs from the IEEE-488 interface bus override the pushbutton selections in the remote mode.

IEEE-488 Interface Assembly A3 provides two-way communications between the Frequency Counter and an instrumentation bus. Data is transferred across the interface in 8-bit bytes. Commands to the instrument set its input range, attenuation and resolution. Measurement data from the instrument is output to the bus in a 15-byte message format. The Frequency Counter responds only to bus inputs specifically addressed to it. The 5-bit instrument address is switch selectable on Assembly A3. A TALK ONLY mode can be selected, where measurement data is output to the bus but input commands are not processed.

4.2.5 Display

Display Assembly A4 contains an 8-digit LED array and 11 status indicators. The count data is sent to the 8-digit LED array in 7-segment format. The scan sequence is left to right, MSD to LSD. Leading zeros are suppressed. Off scale readings (count exceeds the 8-digit display) are denoted by lighting the O.S. indicator.

The MHz and kHz indicators on the front panel denote the input channel selected. Selecting A INPUT lights the kHz indicator and digits to the left of the decimal point are read as kHz. Selecting B INPUT lights the MHz indicator and digits to the left of the decimal point are read as MHz. The decimal point position is a function of both input and resolution selections. (See Table 4-2.)

TABLE 4-2 DECIMAL POINT POSITION MATRIX

INPUT CHANNEL	RESOLUTION (Hz)	DISPLAY FORMAT
A	0.1	M k k k.H H H h
A	1	M M k k k.H H H
A	10	M M M k k k.H H
A	100	- M M M k k k.H
A	1000	- - M M M k k k.
B	0.1	M.k k k H H H h
B	1	M M.k k k H H H
B	10	M M M.k k k H H
B	100	G M M M.k k k H
B	1000	- G M M M.k k k

h = 0.1 Hz M = MHz
H = Hz G = GHz
k = kHz - = suppressed zero

The GATE indicator lights when the measurement gate is open (count accumulating). Gate time is a function of the input (A or B) and resolution selected. When counting B INPUT signals, gate time is extended by a factor of 4 (6042A) or 16 (6043A) to compensate for the prescaling (÷4/÷16) in the A1 Assembly. Table 4-3 defines the gate times by model.

TABLE 4-3 GATE TIME MATRIX

Resolution	A Input all Models	B Input 6042A	B Input 6043A
0.1 Hz	10 sec	40 sec	160 sec
1 Hz	1 sec	4 sec	16 sec
10 Hz	100 ms	400 ms	1600 ms
100 Hz	10 ms	40 ms	160 ms
1000 Hz	1 ms	4 ms	16 ms

The status indicators to the left of the 8-digit LED array define the instruments bus address and mode. A lit

indicator denotes a logical "1". Bit 5 is the MSB of the address. The REMOTE indicator is lit whenever the bus has control of the Frequency Counter. When TALK ONLY is lit, the instrument outputs measurement data to the bus but does accept commands from the bus.

4.2.6 Power

AC power to the Frequency Counter is controlled by the front panel POWER switch. Fuse F1 in the switched side of the ac line prevents the instrument from drawing excessive current (.375A at 115 Vac /.250A at 230 Vac). Transformers T1 and T2 provide stepped down ac to the power supply circuitry on the A2 and A3 Assemblies.

4.3 CIRCUIT DESCRIPTION

The following circuit level descriptions are presented in assembly number order (A1 - A4) for quick reference. The schematic diagrams referenced in the following paragraphs are in Chapter 7. IC (Integrated Circuit) type numbers are listed in tabular form on the schematics. IC data sheets are contained in Chapter 5.

4.4 512 MHz PRESCALER (A1) ASSEMBLY

The following discussion applies to Model 6042A Frequency Counters only. Refer to Figure 7-8. The 512 MHz Prescaler Assembly A1 provides signal conditioning for the B INPUT channel on the 6042A.

The assembly contains four linear amplifier stages, a ÷4 prescaler IC and a comparator circuit used to set B INPUT sensitivity. The input to A1 is protected from signal overload damage by an integral fuse within front panel BNC connector J1.

Prescaler U1 divides the B INPUT by four, and outputs 25-128 MHz to Logic Assembly A2. When B INPUT is selected, the counters timebase is extended X4 to compensate for the prescaling by U1. Extending the timebase to compensate for prescaling normalizes the the Frequency Counters output/ display to Hz.

The B INPUT channel sensitivity is determined by the reference applied to comparator U2, pin 2. The reference is set via sensitivity adjustment R19. If the B INPUT signal level at the collector of Q4 is less than the sensitivity threshold (set by R19) the output at U2-7 turns Q5 on. Q5 clamps the output of prescaler U1 to ground, disabling the B INPUT channel. When the B INPUT level exceeds the threshold point, U2 turns Q5 off and the output of prescaler U1 is counted by Assembly A2.

4.5 1.25 GHz Prescaler (A1) Assembly

The following discussion applies to Model 6043A Frequency Counters only. Refer to Figure 7-10. The 1.25 GHz Prescaler Assembly A1 provides signal conditioning for the B INPUT channel on the 6043A.

The assembly contains four linear amplifier stages, two ÷4 prescaler ICs and a comparator circuit used to set B INPUT sensitivity. The input to A1 is protected from signal overload damage by an integral fuse within front panel BNC connector J1.

Prescalers U1 and U2 are divide by four counters, dividing the B INPUT by 16. Assembly A1 outputs 6.25 to 78.2 MHz to Logic Assembly A2. When B INPUT is selected, the counters timebase is extended X16 to compensate for the prescaling by U1 and U2. Extending the timebase to compensate for prescaling normalizes the Frequency Counters output/display to Hz.

The B INPUT channel sensitivity is determined by the reference applied to comparator U3, pin2. The reference is set via sensitivity adjustment R22.

If the B INPUT signal level at the collector of Q4 is less than the sensitivity threshold (set by R22) the output at U3-7 turns Q5 on. Q5 clamps the output of prescaler U2 to ground, disabling the B INPUT channel. When the B INPUT level exceeds the threshold point, U3 turns Q5 off and the output of prescaler U2 is counted by Assembly A2.

4.6 LOGIC (A2) ASSEMBLY

Refer to Figures 4-2 and 7-12 for the following discussion. Logic Assembly A2 generates the Frequency Counters timebase, counts the selected input signal (A or B) and outputs the count data to IEEE-488 Interface Assembly A3 and Display Assembly A4. Control inputs to Assembly A2 are from the front panel pushbuttons (local) or from the instrumentation bus via Assembly A3 (remote).

4.6.1 Timebase/Gate Time Logic

The Frequency Counters accuracy is a function of measurement gate time accuracy, which is derived from a timebase oscillator, The 604XA series Frequency Counters use an internal 10 MHz Temperature Compensated Crystal Oscillator (TCXO) to drive the gate time logic. A high stability TCXO (option 8) is available for increased accuracy/stability.

An external 1 MHz frequency standard can be substituted for the internal TCXO. Connecting an external 1 MHz standard to J3 triggers one-shot U32, which gates U33 to block the TCXO output and pass the external input signal. If the external signal falls below the retrigger rate of U32, U33 blocks the external input and passes the TCXO output.

The TCXO output is divided by 10 by U31. The output at U33-8 is always 1 MHz, ±any error in the TCXO or the external standard.

Timebase select logic outputs a $\overline{CLK}$ determined by the frequency range (A or B) selected. U30 divides the 1 MHz input by 10. U28 then divides 100 kHz by 4 (6052A) or 16 (6043A). The appropriate output of U28 is hard-wired for ÷4/÷16, depending on the Frequency Counter model. U24 selects the output of U30 (A INPUT selected) or U28 (B INPUT selected) as $\overline{CLK}$. The following truth table applies.

	6041A	6042A	6043A
A INPUT	100 kHz	100 kHz	100 kHz
B INPUT	———	25 kHz	6.25 kHz

A divider chain consisting of U23, U26 and U27 provides five outputs corresponding to the five resolution selections. Data selector U25 selects the appropriate resolution step, based on the 3-bit address input. A high output at U25-14 initiates end of gate time. Gate time ranges from 1 ms to 160 sec., depending or input range (A or B), resolution and model (see Table 4-3).

4.6.2 A INPUT Attenuator

A INPUT signals from front panel connector J2 are terminated by a three step attenuator (X1, X10, X100). The attenuator setting is driven by the A INPUT ATTENUATION pushbuttons (front panel) or by programming inputs from the instrumentation bus. AND gate U1 energizes/de-energizes sections of relay K1, switching in the appropriate resistors. A low (0) out of U1 will energize the relay winding. The following truth table applies.

Attenuation	U1-3	U1-5
X1	H	H
X10	L	H
X100	L	L

The attenuated A INPUT signal drives a signal conditioning circuit consisting of current source Q1 and Q2 and quad line receiver U29. The line

receiver functions as a schmitt trigger, providing enhanced noise immunity. Balance adjustment R59 sets the sensitivity of the A INPUT channel.

4.6.3 Input Select and Gating

Input channel selection (A or B) and gating is provided by quad NOR gate U12. The output of U12 drives BCD counter U5. U12 is enabled during measurement gate time, passing the selected input (A or B) to the counting circuitry.

The AND output at U17-15 enables/disables the A INPUT signal path through U12 to BCD counter U5. The NAND output at U17-12 enables/disables the B INPUT path. Only A or B will be enabled, never both. A high control input disables the applicable NOR gate of U12. The following truth table applies.

Input Selected	U2-6	U17-15	U17-12
A	L	L	H
B	H	H	L

The start/stop logic out of U13 enables U12 to pass the selected input signal during gate time. The low output from U14-13 lights the GATE indicator on the front panel. At the end of gate time U12 is disabled. The low out of U14-4 indicates end of count ($\overline{EOC}$) to Assembly A3 and triggers the store and reset logic.

4.6.4 Counter Logic

The frequency of an unknown signal is determined by counting the number of transitions during a specified period (gate time). The gated output of U12 drives BCD counter U5, a high speed ECL device. The most significant bit (MSB) out of U5 clocks BCD counter U8, which in turn clocks 6-digit LSI counter U7. Translator U6 converts ECL levels to TTL. At the end of gate time the BCD output of U5 defines the LSD (10^0) of the 8-digit count, while U8 defines the next LSD (10^1). The remaining six digits of the count (10^2-10^7) represent the total number of $\overline{CLK}$ transitions counted during gate time by U7.

At the end of gate time the $\overline{STORE}$ input to U7 freezes the accumulated count. The stored count is then read out to the A3 and A4 Assemblies, at a rate determined by the value of C17. The BCD value of the MSD (10^7) is read out first, followed by the remaining seven digits in decending order (10^6-10^0). The weight of the digit being sent is indicated by driving one of eight position flags low. Transistors Q6 through Q13 send a high enabling signal to each of the eight front panel LEDs, in MSD to LSD sequence. The value (0-9) of each digit is sent to A3 in BCD format, but is converted to 7-segment format to drive the LEDs on Display Assembly A4.

Off scale counts (count exceeds eight digits) are indicated by a high at U7-26. An off scale count turns Q4 on, sending a low to the O.S. indicator on the front panel. The appropriate decimal point on Display Assembly A4 is activated by a low out of Q5 coincident with the appropriate digit in the scan sequence. The decimal point position is determined by the 3-bit input to U7 pins 23, 24 and 25.

4.6.5 Decimal Point Encoding

Decimal point position is a function of the input range and resolution selected (see Table 4-2). NAND gates U2 and U3 encode the resolution selection as follows.

Resolution	U2-8	U3-6	U3-12
0.1 Hz	0	1	1
1 Hz	1	0	0
10 Hz	1	0	1
100 Hz	1	1	0
1000 Hz	1	1	1

The 3-bit resolution code controls one-of-eight data selector U25, determining the measurement gate time. This 3-bit code also addresses PROM U4. A fourth address bit to U4 is low for A INPUT and high for B INPUT signals. A 3-bit output from U4 provides decimal point position information to counter U7 and to IEEE-488 Interface Assembly A3. PROM programming for U4 is shown in Table 4-4.

TABLE 4-4 DECIMAL POINT PROM (A2U4) PROGRAM

Input	Output
E D C B A	8 7 6 5 4 3 2 1
1 0 0 1 1	1 1 0 0 0 0
1 0 1 0 0	1 1 0 0 0 1
1 0 1 0 1	1 1 0 0 1 0
1 0 1 1 0	1 1 0 0 1 1
1 0 1 1 1	1 1 0 1 0 0
1 1 0 1 1	0 0 1 0 1 1
1 1 1 0 0	0 0 1 1 0 0
1 1 1 0 1	0 0 1 1 0 1
1 1 1 1 0	0 0 1 1 1 0
1 1 1 1 1	0 0 1 1 1 1

Input E is hardwired high.
Output 5 lights kHz indicator (low).
Output 6 lights MHz indicator (low).
Output 8 selects $\overline{CLK}$ rate.

4.7 IEEE-488 INTERFACE (A3) ASSEMBLY

Refer to Figures 4-3 and 7-14 for the following discussion. IEEE-488 Interface Assembly A3 provides two-way communications between the 604XA series Frequency Counter and an instrumentation bus. Data is transferred across the interface in 8-bit bytes (bit 8 [MSB] is always logic 0 on the bus). In addition to the eight data lines, five interface management lines and three data transfer control (handshake) lines control bus functions. By definition, the bus uses negative true logic, levels ≤+.8V denoting a logic 1, while levels ≥ +2V denote a logic 0.

4.7.1 Bus Transceivers

Three quad bus transceivers provide input/output multiplexing for 12 of 16 bus lines. The receive side of the transceiver buffers data on the bus into Assembly A3. The send side consists of OR gates with a common enable line. The send function is enabled when $\overline{TALK}$ is low, routing data out of A3 and onto the bus.

Four of the 16 bus lines are not routed through the transceiver. REN (Remote Enable) is always an input and is tied to U8-9. EOI, SRQ and DIO8 are not used by the Frequency Counter. They are hardwired high, putting a logic 0 on the bus.

4.7.2 Address Decoding

In a practical instrumentation system each instrument on the bus has a unique address. The 604XA series Frequency Counters are assigned a specific 5-bit address via DIP switch S1 on Assembly A3. Each 5-bit combination represents both a send (talk) and a receive (listen) address. Table 3-4 defines the range of addresses. Note that 1 1 1 1 1 is not a valid address.

The Frequency Counter only responds to programming inputs intended for its assigned listen address. Address comparator U17 compares DI1-DI5 with the five address switches (S1) and outputs a high ADD COMP when a match occurs.

The instruments assigned address can be changed by setting a new address code into DIP switch S1.

4.7.3 Program Input Decoder

Programming inputs from the instrumentation bus set the Frequency Counter input range, attenuation factor and resolution. The state of HOLD/RECYCLE and SAMPLE/RESET are also programmable via the bus. Table 3-6 defines the program format. The four bytes of

programming data can be entered in any order. If any or all of the first three programming bytes are omitted, the Frequency Counter will default to the "wake up" states defined in Table 3-6. Programming inputs over ride the front panel control settings (except POWER) when the Frequency Counter is in REMOTE. The decoded programming commands are output at A3J4 and routed to A2J4.

Resolution commands are sent as program byte one and are decoded by flip flops U30 and U31, and BCD to decimal decoder U36. The MSB of the 4-bit input to U36 (pin 12) must be low. This condition is satisfied when REMOTE is low. U36 outputs a low on the selected resolution line to Logic Assembly A2, where it determines gate time and decimal point position. If no resolution selection (byte one) is sent, the Frequency Counter will wake up (default) to 0.1 Hz.

Range (A or B) and attenuation commands are sent as program byte two and are decoded by flip flop U40, AND gate U39 and NAND gate U37. A common enable input to the four NAND gates (U37) is satisfied when REMOTE in low. Only one of the four outputs from U37 can be low at any given time. If no range/attenuation selection (byte two) is sent, the Frequency Counter will wake up (default) to A INPUT X10.

Program byte three selects either the HOLD or RECYCLE mode. In the HOLD mode only one measurement is taken, then held until a reset is sensed. In the RECYCLE mode repetitive measurements are taken. If no HOLD/RECYCLE selection (byte three) is sent, the Frequency Counter will wake up (default) to HOLD.

Program byte four determines the SAMPLE/RESET state. SAMPLE and RESET are mutually exclusive. Only one of these two outputs to Assembly A2 can be low at any given time.

4.7.4 IEEE-488 Interface Logic

Data transfer across the bus/instrument interface is controlled by the interface logic circuitry. Inputs include seven data lines (DI1-DI7), three interface management lines (ATN, IFC, REN) and the three handshake lines (DAV, NRFD, NDAC). In addition, control signals generated on Assembly A3 provide inputs to the interface logic circuitry. TALK ONLY disables the listen function. ADD COMP goes high when the listen address on the bus corresponds to the instruments assigned listen address. EOC goes high to indicate end of count, thereby initiating the measurement output sequence. A low 12-15 indicates that the 8-digit count has been sent and exponent sign, exponent value or delimiter bytes are being sent.

Outputs from the interface logic circuitry control the transceivers send/receive mode, generate the appropriate handshake responses and control the count data output sequence. A low TALK enables the bus transceiver send side, outputting data onto the bus. The three handshake outputs; DAV OUT, RFD OUT and DAC OUT are sent in response to the DAV, NRFD and NDAC inputs in accordance with IEEE-488 protocol. STEP RESET clears the measurement output encoder. STEP clocks the output encoder through the 15 byte output sequence.

4.7.5 Measurement Output Encoder

The 604XA Series Frequency Counters output measurement data to the bus in a 15-byte format. Table 3-7 defines the output format. Encoder inputs (from A2) include a 4-bit BCD representation of each digit, a one-of-eight input that defines the digit being sent (10^7- 10^1) and a 3-bit decimal point code. EOC (end of count) and STORE/RESET inputs from A2 control the encoder functions (load/read out). The STEP input clocks the encoder through the 15-byte output sequence.

$\overline{\text{STEP}}$ $\overline{\text{RESET}}$ clears the encoder for the next measurement input from Assembly A2.

The 8-digit count from Assembly A2 is loaded into RAM U3. The eight digits are stored in BCD format, J2-13 being the MSB. The eight memory locations within U3 are specified by a 3-bit address input from U5. During the load sequence U5-1 is low, and the A input of U5 is routed to U3 as its address input. The address sent to U3 is a function of which digit (10^7 through 10^0) is being input from A2. U13 senses which one of eight inputs is high, corresponding to which digits BCD value is being sent. The scan sequence is 10^7 to 10^0, MSD to LSD. During the load cycle U3-3 (Write Enable) is held low. The load cycle is terminated when $\overline{\text{EOC}}$ (U9-6) goes low, causing the WE input to U3 to go high. The high output from U9-5 switches U5 to its B inputs.

Once loaded, the 8-digit count, off scale status, exponent sign, exponent value and delimiters are sent to the bus. The sequence of data output to the bus is controlled by byte counter U6. U6 is initialized to output 1101, when $\overline{\text{STEP}}$ $\overline{\text{RESET}}$ to U6-1 goes low. An input address of X1101 to PROM U4 outputs an ASCII LF (line feed) on the bus prior to sending any measurement data. Table 4-5 defines the program loaded in PROM U4. Remember that the instrumentation bus uses negative true logic, therefore the output of U4 is the compliment of any ASCII characters referred to in the following paragraphs.

After being initialized to 1101, byte counter U6 is clocked through the remaining output bytes by $\overline{\text{STEP}}$. Counts 1110 and 1111 out of U6 address U4 to send off scale status to the bus. This corresponds to output bytes 1 and 2 (Table 3-7). If the count is off-scale (exceeds eight digits) an ASCII 0 (byte 1) and S (byte 2) are put on the bus. If the count is not offscale an ASCII SP (space) is sent out on the bus.

TABLE 4-5 PROM (A3U4) PROGRAM

Input					Output								Function/ Message
E	D	C	B	A	8	7	6	5	4	3	2	1	
0	0	0	0	0	1	1	0	0	1	1	1	1	MSD (10^7)
0	0	0	0	1									
0	0	0	1	0									
0	0	0	1	1									
0	0	1	0	0									
0	0	1	0	1									
0	0	1	1	0									
0	0	1	1	1	1	1	0	0	1	1	1	1	LSD (10^0)
0	1	0	0	0	1	0	1	1	1	0	1	0	E
0	1	0	0	1	1	1	0	1	0	0	1	0	–
0	1	0	1	0	0	1	0	0	1	1	1	1	(EXPONENT #)
0	1	0	1	1	1	1	1	1	0	0	1	0	CR
0	1	1	0	0	1	1	1	1	0	1	0	1	LF
0	1	1	0	1	1	1	1	1	0	1	0	1	LF
0	1	1	1	0	1	0	1	1	0	0	0	0	0
0	1	1	1	1	1	0	1	0	1	1	0	0	S
1	0	0	0	0	1	1	0	0	1	1	1	1	MSD (10^7)
1	0	0	0	1									
1	0	0	1	0									
1	0	0	1	1									
1	0	1	0	0									
1	0	1	0	1									
1	0	1	1	0									
1	0	1	1	1	1	1	0	0	1	1	1	1	LSD (10^0)
1	1	0	0	0	1	0	1	1	1	0	1	0	E
1	1	0	0	1	1	1	0	1	0	1	0	0	+
1	1	0	1	0	0	1	0	0	1	1	1	1	(EXPONENT #)
1	1	0	1	1	1	1	1	1	0	0	1	0	CR
1	1	1	0	0	1	1	1	1	0	1	0	1	LF
1	1	1	0	1	1	1	1	1	0	1	0	1	LF
1	1	1	1	0	1	1	0	1	1	1	1	1	SP
1	1	1	1	1	1	1	0	1	1	1	1	1	SP

BCD values for digits 10^7-10^0 are from A3U3 output.
Exponent value is from A3U2 output.

The next eight counts out of U6 (0000-0111) address RAM U3 (via U5) to read out the BCD values of the eight digit count. The read function of U3 is

enabled by a low to pin 2. The count is read out to the bus in an MSD (10^7) to LSD (10^0) sequence. This corresponds to output bytes 3-10 (Table 3-7)

The next count out of U6 (1000) disables U3 with a high to pin 2, and addresses U4 to put an ASCII E on the bus. See Table 3-7, byte 11.

Output byte 12 sends the sign of the exponent. Output byte 13 sends the value of the exponent, which is a function of the range and resolution selected. PROM U2 outputs an exponent value determined by decimal point position and range (A or B). Table 4-6 defines the program for PROM A3U2. U2 is enabled during byte 13 by a low on U2-15.

Bytes 14 and 15 are delimiters used to advance a printer on the bus or otherwise signify that the complete measurement data (15 bytes) has been sent.

TABLE 4-6 PROM (A3U2) PROGRAM

Input	Output	Function
E D C B A	8 7 6 5 4 3 2 1	
* 0 0 1 1	0 0 0 0 0 1 0 0	Exp = 3
0 1 0 0	1 0 1	2
0 1 0 1	1 1 0	1
0 1 1 0	1 1 1	0
0 1 1 1	1 1 0	1
1 0 0 0	1 0 0	Exp = 3
1 0 0 1	1 0 1	2
1 0 1 0	1 1 0	1
1 0 1 1	1 1 1	0
* 1 1 0 0	0 0 0 0 0 1 1 0	1

Input E to U2 is hardwired low.
Compliment the three least significant bits to obtain the true exponent number.
Input D is low when B INPUT is selected.

4.8 DISPLAY (A4) ASSEMBLY

Refer to Figure 7-16 for the following discussion. The front panel contains eight 7-segment LED's (to display the count) and 11 status indicators.

The digit (0-9) to be displayed is sent to the eight LED's in 7-segment format (see Table 4-7). A low input lights the corresponding segment.

TABLE 4-7 7-SEGMENT DRIVE FORMAT

Input A B C D E F G	Digit Displayed
L L L L L L H	0
H L L H H H H	1
L L H L L H L	2
L L L L H H L	3
H L L H H L L	4
L H L L H L L	5
L H L L L L L	6
L L L H H H H	7
L L L L L L L	8
L L L H H L L	9
A low input lights the corresponding segment.	

The eight 7-segment LED's are enabled sequentially, DS8 to DS1, by a high on pin 14. The 7-segment input is changed at the scan rate, as each LED is enabled right to left across the display. The scan rate is determined by the LSI counter (U7) on Logic Assembly A2.

The decimal point is enabled by a low input to J3-16. The decimal point position in the display is a function of when it is enabled during the scan sequence. Table 4-2 defines the decimal point position for range and resolution selections.

Four of the 11 front panel status indicators provide the instrument user with visual reminders of range

selected (DS17/DS16), measurement gate status (DS18) and off scale status (DS19). These indicators are turned on by a low input to the appropriate pin of J3 from Logic Assembly A2.

Instrumentation bus mode (DS14, DS15) and the instruments bus address (DS9-DS13) are indicated by the remaining seven status indicators. These LED indicators are turned on by a low to the appropriate pin on J1 from IEEE-488 Interface Assembly A3.

TABLE 4-8 WIRE LIST (1) A3/A4

A3J1 pin#	A4J1 pin#	SIGNAL/FUNCTION	
1	1	ADD BIT 1 (LSB)	RTN
2	2	TALK ONLY	RTN
3	3	ADD BIT 2	RTN
4	4	+5	
5	5	ADD BIT 3	RTN
6	6		
7	7	ADD BIT 4	RTN
8	8		
9	9	ADD BIT 5 (MSB)	RTN
10	10	REMOTE	RTN
11	11	REMOTE	+5
12	12	ADD BIT 5	+5
13	13		
14	14	ADD BIT 4	+5
15	15		
16	16	ADD BIT 3	+5
17	17	+5	
18	18	ADD BIT 2	+5
19	19	TALK ONLY	+5
20	20	ADD BIT 1	+5

TABLE 4-9 WIRE LIST (2) A2/A3

A2J2 pin#	A3J2 pin#	SIGNAL/FUNCTION
1	1	$\overline{\text{STORE}}$ OR $\overline{\text{RESET}}$
2	2	OFF SCALE
3	3	10^6 LED ENABLE
4	4	10^1 LED ENABLE
5	5	10^7 LED ENABLE (MSD)
6	6	10^5 LED ENABLE
7	7	10^3 LED ENABLE
8	8	10^2 LED ENABLE
9	9	10^0 LED ENABLE (LSD)
10	10	BCD 2^2
11	11	10^4 LED ENABLE
12	12	BCD 2^3
13	13	BCD 2^4
14	14	GND
15	15	DECIMAL POINT 2^1
16	16	BCD 2^1
17	17	DECIMAL POINT 2^3
18	18	DECIMAL POINT 2^2
19	—	
20	20	$\overline{\text{EOC}}$

TABLE 4-10 WIRE LIST (3) A2/A4

A2J3 pin#	A4J3 pin#	SIGNAL/FUNCTION
1	1	$\overline{10^7}$ LED ENABLE (MSD)
2	2	$\overline{G}$
3	3	$\overline{10^5}$ LED ENABLE
4	4	$\overline{C}$
5	5	$\overline{D}$
6	6	$\overline{E}$
7	7	$\overline{A}$ SEG
8	8	$\overline{B}$
9	9	$\overline{10^1}$ LED ENABLE
10	10	$\overline{10^0}$ LED ENABLE (LSD)
11	11	$\overline{\text{kHz LITE}}$
12	12	$\overline{\text{MHz LITE}}$
13	13	$\overline{10^2}$ LED ENABLE
14	14	$\overline{10^3}$ LED ENABLE
15	15	$\overline{F}$
16	16	$\overline{\text{DP}}$ (DECIMAL POINT)
17	17	$\overline{10^4}$ LED ENABLE
18	18	$\overline{10^6}$ LED ENABLE
19	19	$\overline{\text{GATE LITE}}$
20	20	$\overline{\text{O.S.}}$ (OFF SCALE)

TABLE 4-11 WIRE LIST (4) A3/A2

A3J4 pin#	A2J4 pin#	SIGNAL/FUNCTION
1	1	$\overline{\text{GND}}$
2	2	$\overline{\text{LAMP TEST}}$
3	3	$\overline{\text{SAMPLE}}$
4	—	+5V IN
5	5	$\overline{\text{RESET}}$
6	6	$\overline{\text{X100}}$
7	7	$\overline{\text{X1}}$
8	8	$\overline{\text{X10}}$
9	9	$\overline{\text{1 kHz}}$
10	10	$\overline{\text{100 Hz}}$
11	11	HOLD
12	12	$\overline{B}$
13	13	$\overline{\text{10 Hz}}$
14	14	$\overline{\text{1 Hz}}$
15	15	$\overline{\text{.1 Hz}}$
16	16	$\overline{\text{RESET}}$
17	17	$\overline{\text{REMOTE}}$
18	18	$\overline{\text{SAMPLE}}$
19	19	$\overline{\text{LAMP TEST}}$
20	20	GND

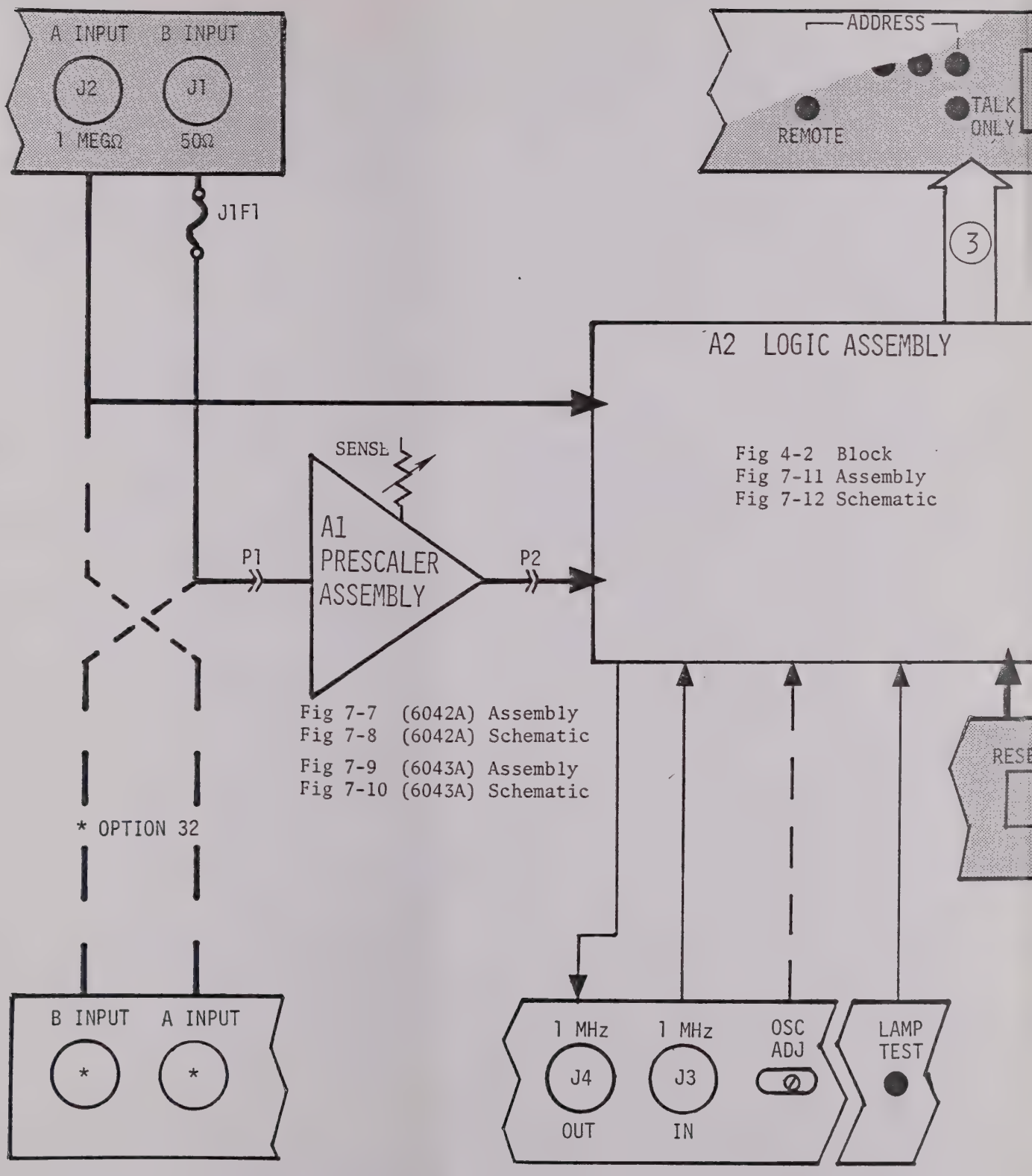


Fig 4-2 Block
Fig 7-11 Assembly
Fig 7-12 Schematic

Fig 7-7 (6042A) Assembly
Fig 7-8 (6042A) Schematic
Fig 7-9 (6043A) Assembly
Fig 7-10 (6043A) Schematic

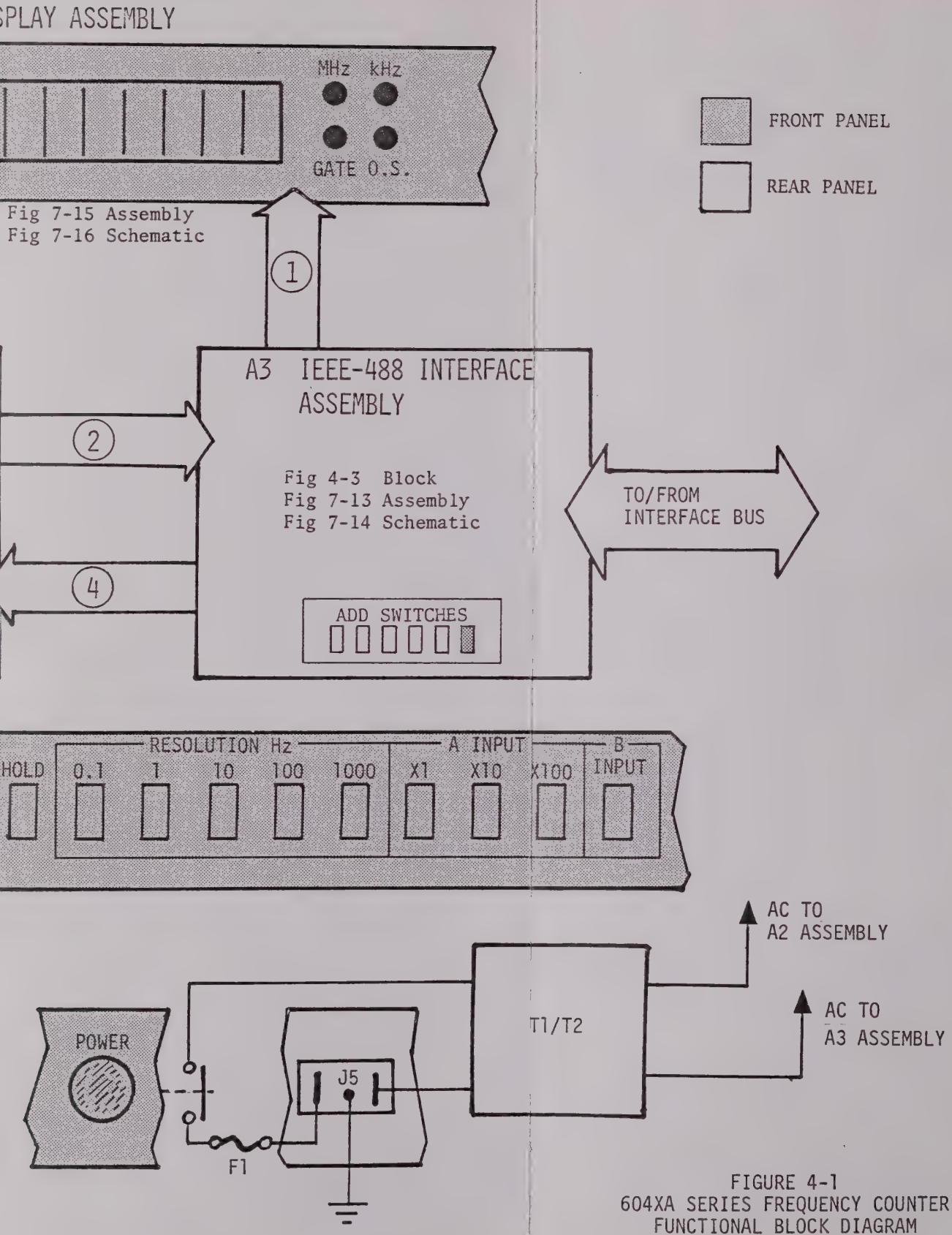
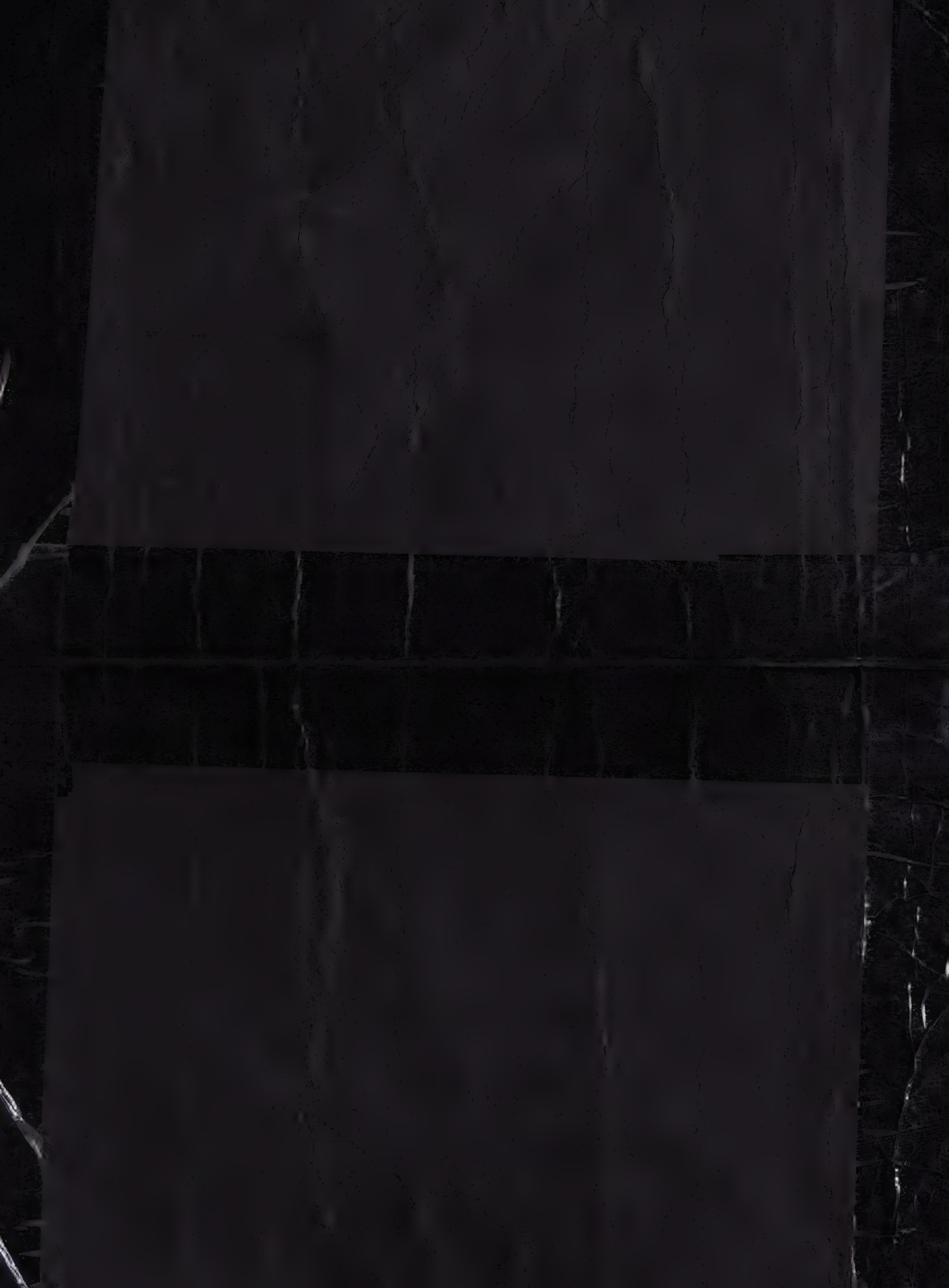


FIGURE 4-1
604XA SERIES FREQUENCY COUNTER
FUNCTIONAL BLOCK DIAGRAM



(1) TABLE 4-1 604XA SERIES FREQUENCY COVERAGE

Model	A INPUT (J2)	B INPUT (J1)
6041A	20 Hz - 100 MHz	Not Used
6042A	20 Hz - 100 MHz	100 MHz - 512 MHz
6043A	20 Hz - 100 MHz	100 MHz - 1.25 GHz

(2) TABLE 4-3 GATE TIME MATRIX

Resolution	A Input all Models	B Input 6042A	B Input 6043A
0.1 Hz	10 sec	40 sec	160 sec
1 Hz	1 sec	4 sec	16 sec
10 Hz	100 ms	400 ms	1600 ms
100 Hz	10 ms	40 ms	160 ms
1000 Hz	1 ms	4 ms	16 ms

(3) TABLE 4-4 DECIMAL POINT PROM (A2U4) PROGRAM

Input	Output
E D C B A	8 7 6 5 4 3 2 1
1 0 0 1 1	1 1 0 0 0 0
1 0 1 0 0	1 1 0 0 0 1
1 0 1 0 1	1 1 0 0 1 0
1 0 1 1 0	1 1 0 0 1 1
1 0 1 1 1	1 1 0 1 0 0
1 1 0 1 1	0 0 1 0 1 1
1 1 1 0 0	0 0 1 1 0 0
1 1 1 0 1	0 0 1 1 0 1
1 1 1 1 0	0 0 1 1 1 0
1 1 1 1 1	0 0 1 1 1 1

Input E is hardwired high.
Output 5 lights kHz indicator (low).
Output 6 lights MHz indicator (low).
Output 8 selects $\overline{\text{CLK}}$ rate.

(4) TABLE 4-2 DECIMAL POINT POSITION MATRIX

INPUT CHANNEL	RESOLUTION (Hz)	DISPLAY FORMAT
A	0.1	M k k k.H H H h
A	1	M M k k k.H H H
A	10	M M M k k k.H H
A	100	- M M M k k k.H
A	1000	- - M M M k k k.
B	0.1	M.k k k H H H h
B	1	M M.k k k H H H
B	10	M M M.k k k H H
B	100	G M M M.k k k H
B	1000	- G M M M.k k k

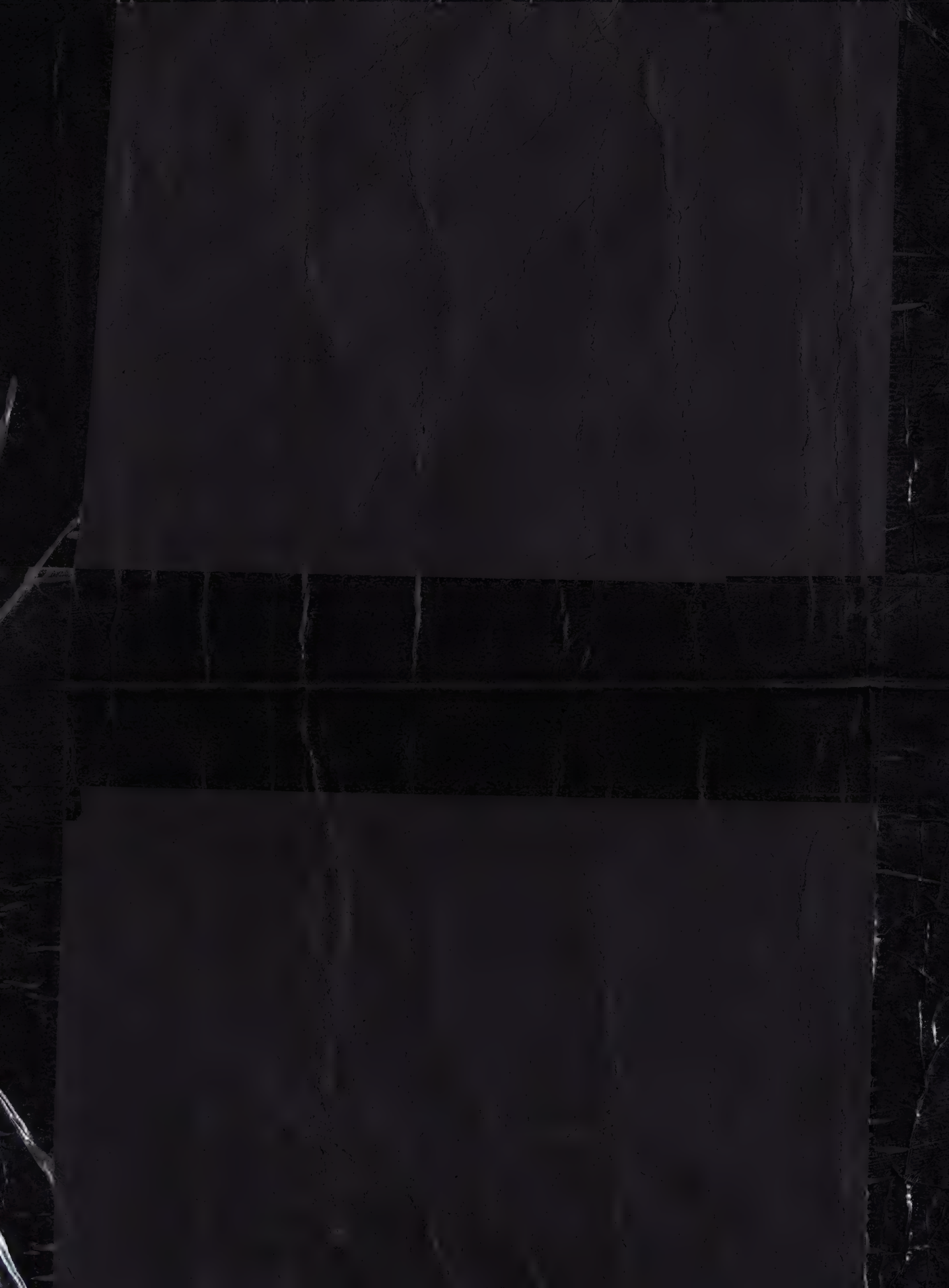
h = 0.1 Hz M = MHz
H = Hz G = GHz
k = kHz - = suppressed zero

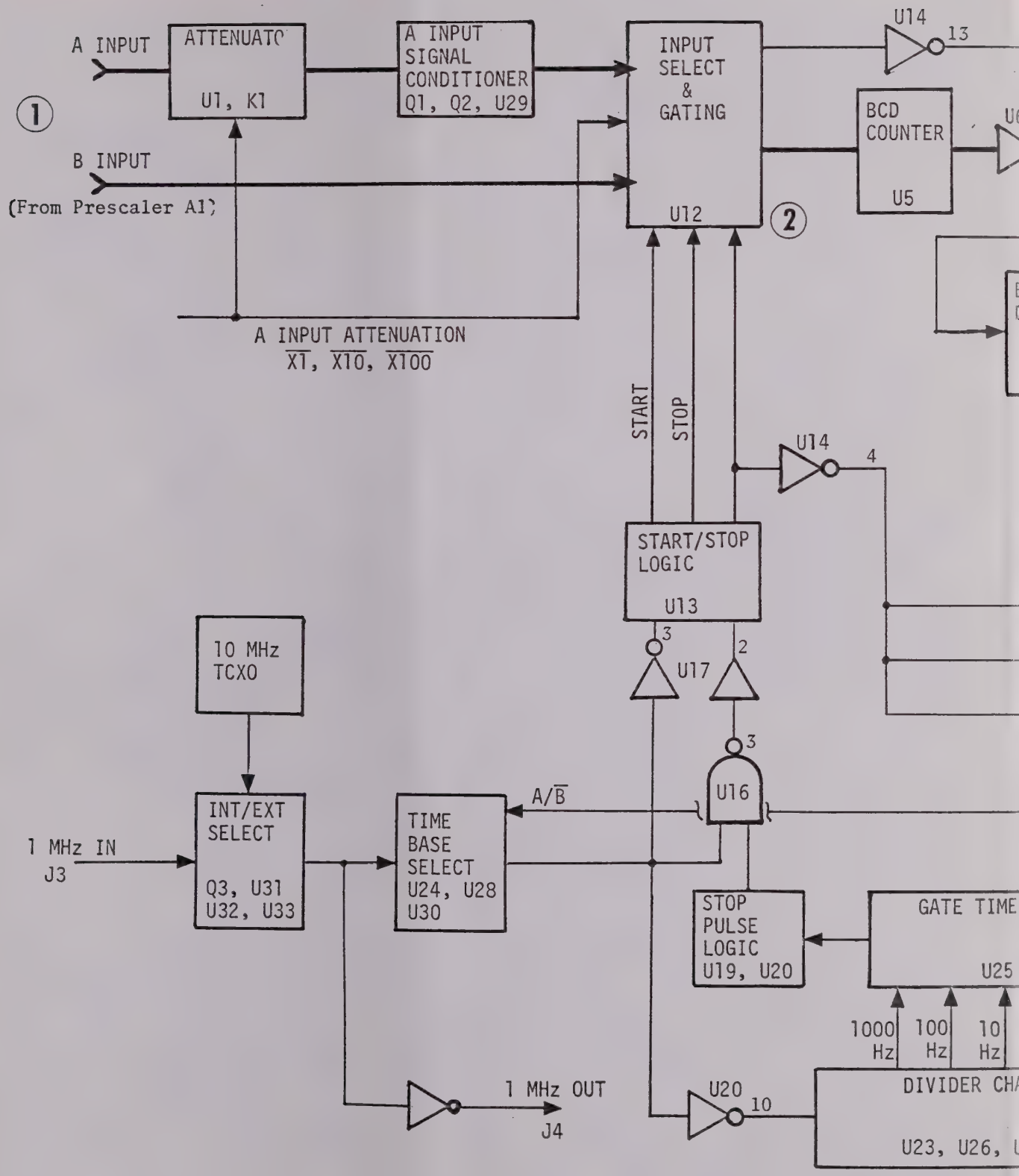
(5) TABLE 4-7 7-SEGMENT DRIVE FORMAT

Input A B C D E F G	Digit Displayed
L L L L L L H	0
H L L H H H H	1
L L H L L H L	2
L L L L H H L	3
H L L H H L L	4
L H L L H L L	5
L H L L L L L	6
L L L H H H H	7
L L L L L L L	8
L L L H H L L	9

A low input lights the corresponding segment.

NOTE: Tables reproduced here for quick refernece.




A INPUT
ATTENUATO
U1, K1
A INPUT
SIGNAL
CONDITIONER
Q1, Q2, U29
INPUT
SELECT
&
GATING
U12
U14
13
BCD
COUNTER
U5
1
2
B INPUT
(From Prescaler A1)
A INPUT ATTENUATION
X1, X10, X100
START
STOP
U14
4
START/STOP
LOGIC
U13
3
2
U17
10 MHz
TCXO
3
U16
A/B
INT/EXT
SELECT
Q3, U31
U32, U33
1 MHz IN
J3
TIME
BASE
SELECT
U24, U28
U30
STOP
PULSE
LOGIC
U19, U20
GATE TIME
U25
1000
Hz
100
Hz
10
Hz
1 MHz OUT
J4
U20
10
DIVIDER CHA
U23, U26,

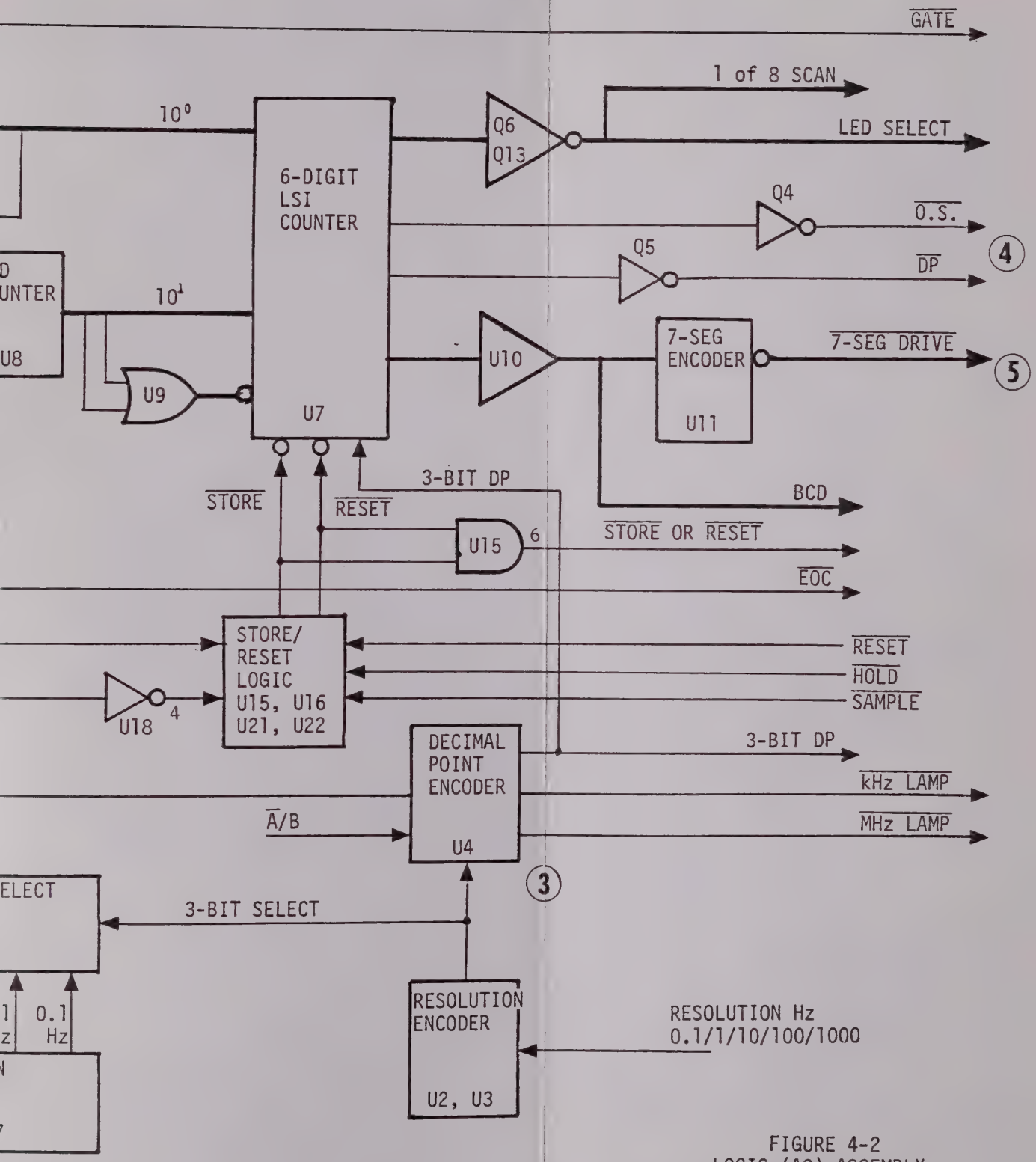
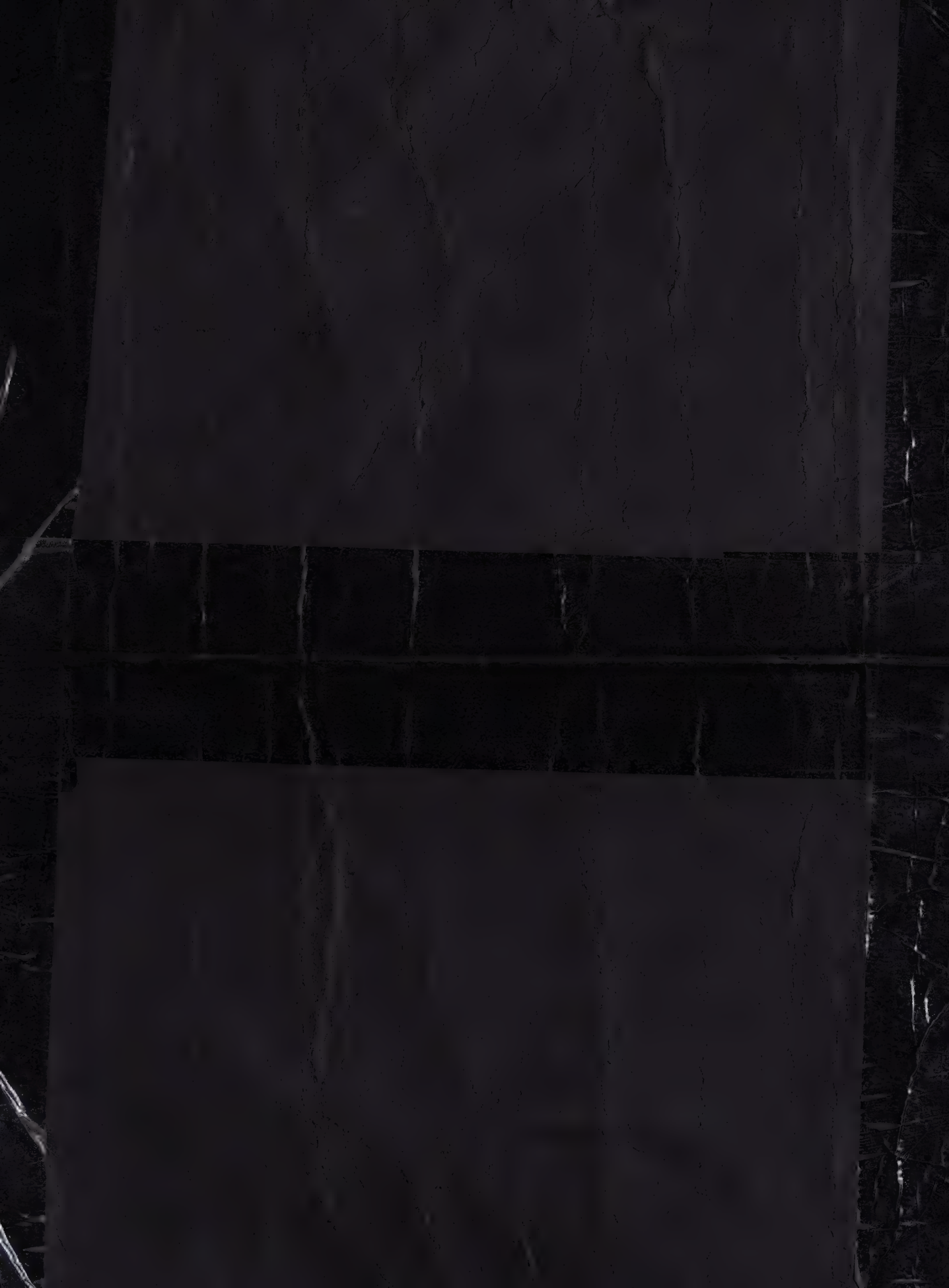


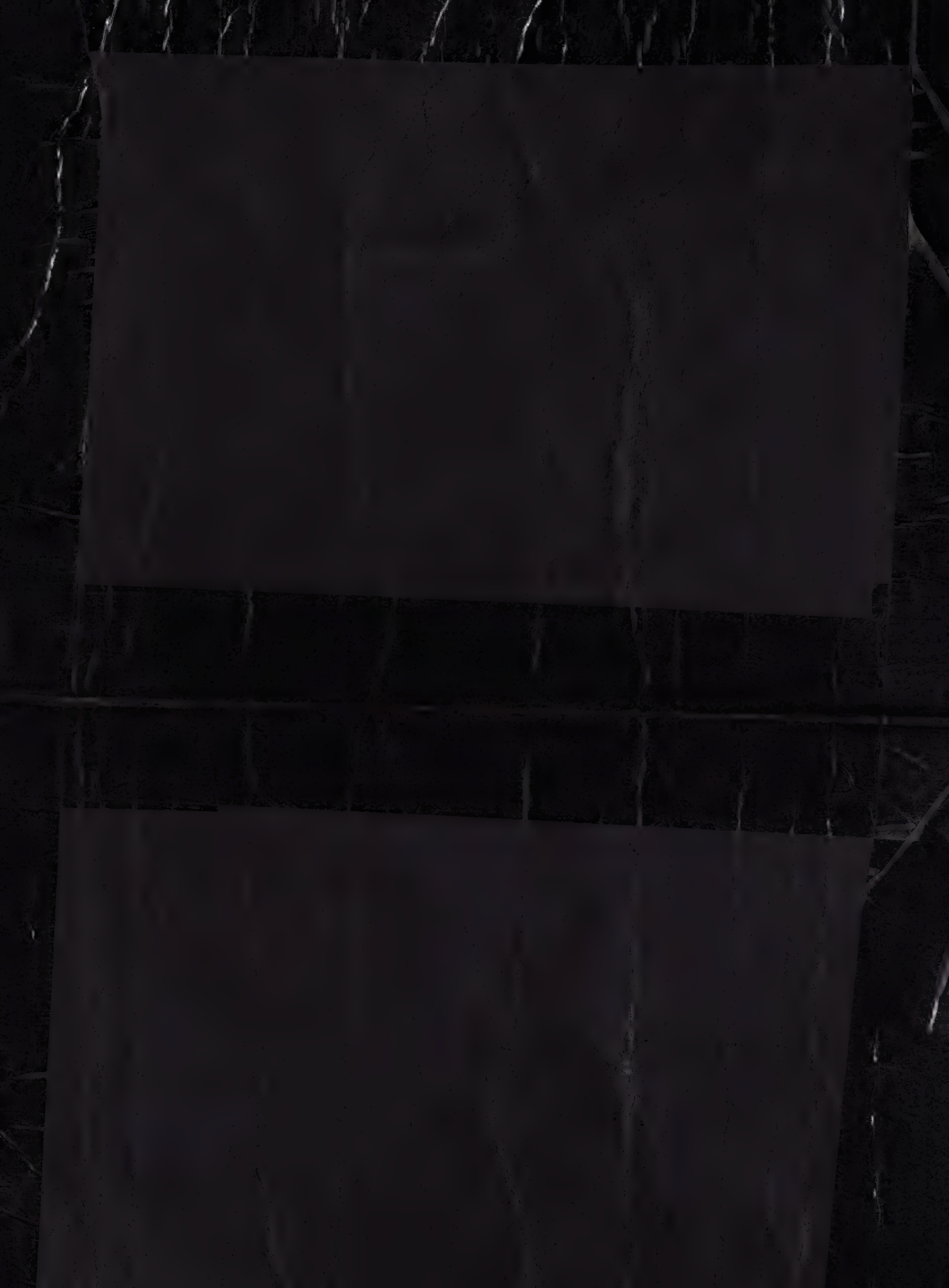
FIGURE 4-2
LOGIC (A2) ASSEMBLY
BLOCK DIAGRAM

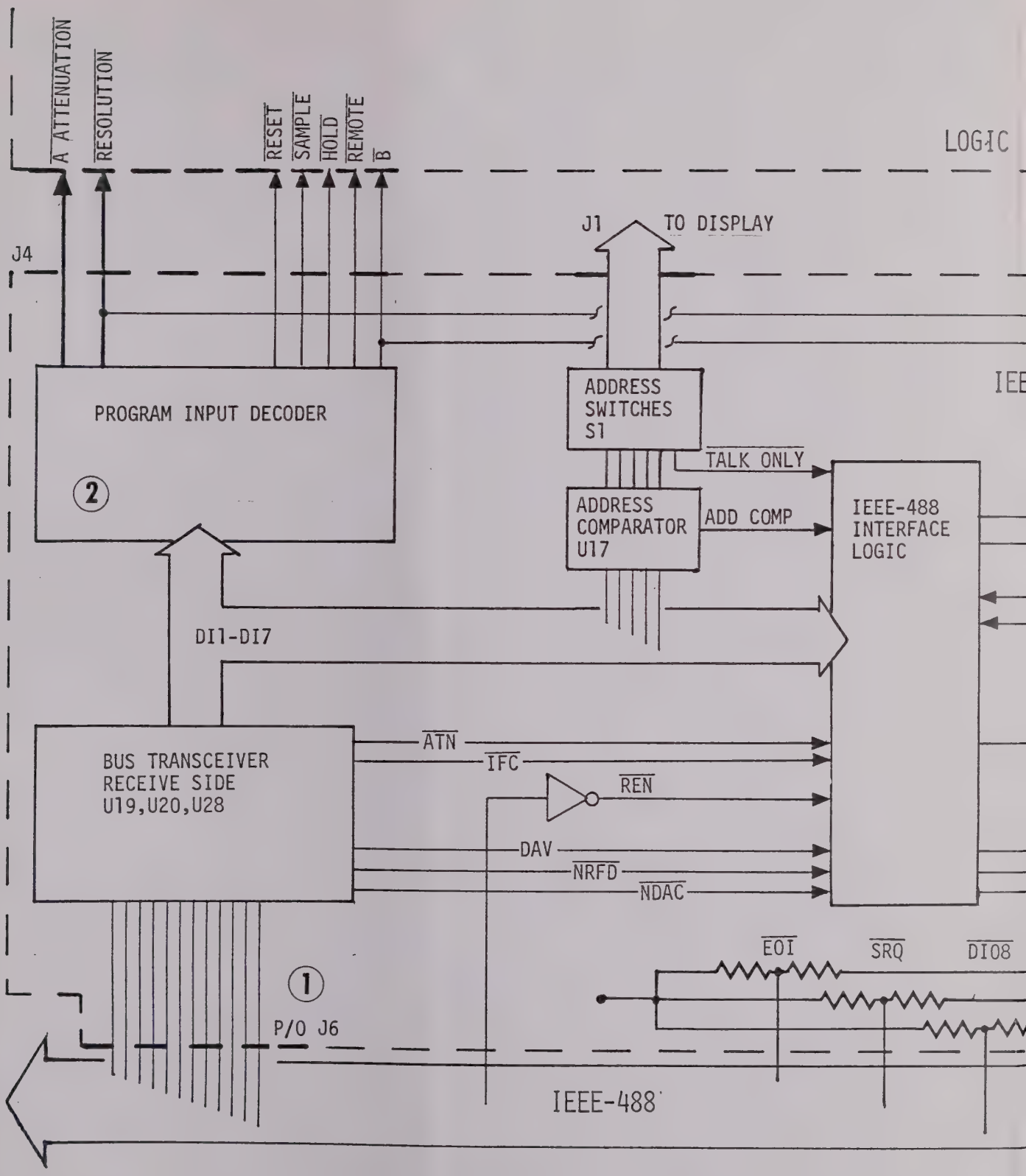


(1) TABLE 2-2 IEEE-488 INTERFACE CONNECTOR

PIN NUMBER	IEEE-488 MNEMONIC
1	DIO1
2	DIO2
3	DIO3
4	DIO4
5	EOI (Inactive)
6	DAV
7	NRFD
8	NDAC
9	IFC
10	SRQ (Inactive)
11	ATN
12	GND (Shield)
13	DIO5
14	DIO6
15	DIO7
16	DIO8 (Inactive)
17	REN
18	GND (Return)
19	GND (Return)
20	GND (Return)
21	GND (Return)
22	GND (Return)
23	GND (Return)
24	GND (Return)

NOTE: Tables reproduced here for quick reference.




A ATTENUATION
RESOLUTION
RESET
SAMPLE
HOLD
REMOTE
B
LOGIC
J4
J1
TO DISPLAY
PROGRAM INPUT DECODER
2
ADDRESS SWITCHES S1
TALK ONLY
ADDRESS COMPARATOR U17
ADD COMP
IEEE-488 INTERFACE LOGIC
DI1-DI7
BUS TRANSCEIVER RECEIVE SIDE U19,U20,U28
ATN
IFC
REN
DAV
NRFD
NDAC
EOI
SRQ
DIO8
1
P/O J6
IEEE-488

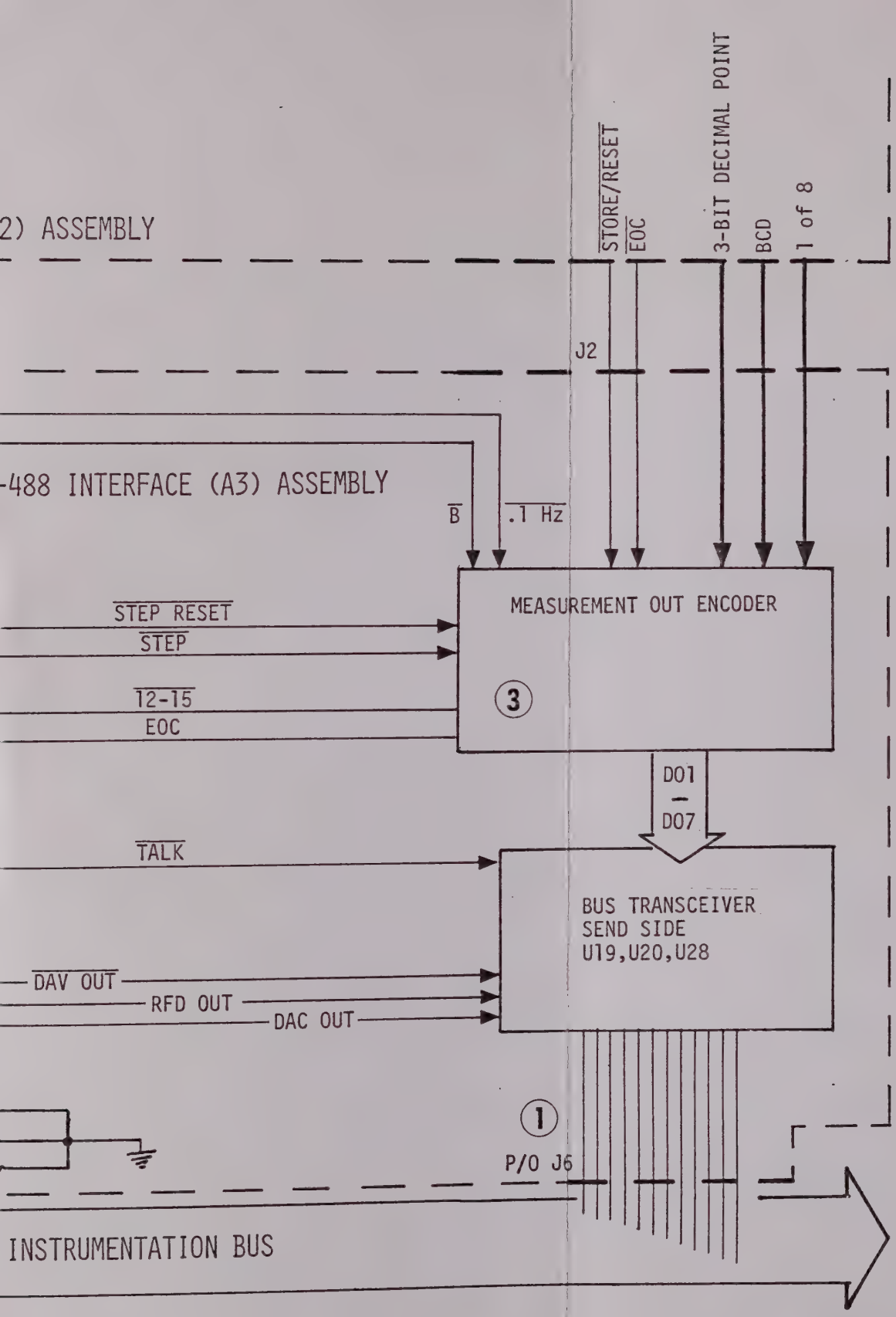


FIGURE 4-3
IEEE-488 INTERFACE (A4) ASSEMBLY
BLOCK DIAGRAM

1. Apply the 1 MHz output of the Frequency Standard to the external trigger connector of the oscilloscope, set the sweep rate to 0.01 µs/cm and select the external trigger mode.

2. Connect the Rear Panel 1 MHz OUT connector to the vertical input of the oscilloscope.

3. Adjust the Rear Panel access OSC ADJ control for a near stationary waveform on the oscilloscope, then readjust for minimum drift of the waveform.

4. Monitor the oscilloscope noting the rate of drift. The amount of error as referenced to the Frequency Standard can be calculated by the drift rate. A

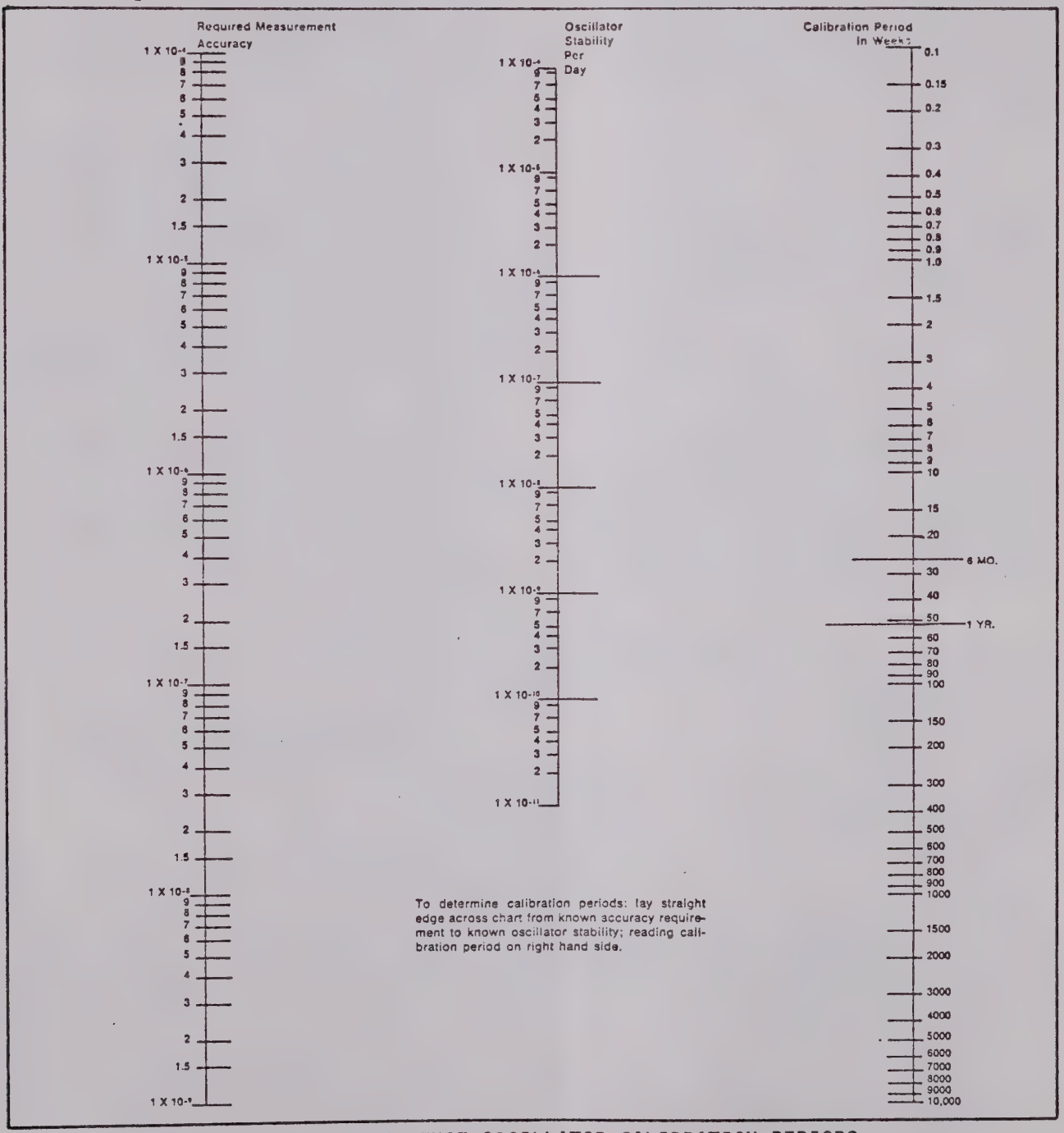


FIGURE 5-1 REFERENCE OSCILLATOR CALIBRATION PERIODS

1 cm/s drift indicates an error of 1 part in 10^{-8} (0.01 PPM).

5.4 CHECKOUT PROCEDURE AND INITIAL CONFIDENCE TEST

1. Ensure that the two Power Transformer (T1 and T2) primaries are wired for the appropriate line voltage and that the appropriate fuse (.375A SLO BLO for 115V or .250A for 230V) is installed in the Rear Panel fuse holder.

2. Apply appropriate ac power to the Rear Panel line power connector and press the Front Panel POWER pushbutton switch.

3. Measure and verify the following voltage regulator outputs.

A2U34 +5V ±.25V (+4.75 to +5.75V)
A2U35 -5.2V ±.25V (-4.95 to -5.4V)
A2U36 -2V ±0.1V (-1.90 to -3.10V)
A3U56 +5V ±.25V (+4.75 to +5.25V)

4. Press A INPUT X1 and RESOLUTION Hz 1000 pushbutton switches, press and hold the Rear Panel LAMP TEST pushbutton switch and verify that the display indicates 88888888, and the REMOTE LED indicator illuminates.

5. Perform the following display readout check by selecting the different INPUT and RESOLUTION combinations.

INPUT CHANNEL	RESOLUTION (Hz)	DISPLAY FORMAT
A	0.1	M k k k.H H H h
A	1	M M k k k.H H H
A	10	M M M k k k.H H
A	100	- M M M k k k.H
A	1000	- - M M M k k k.
B	0.1	M.k k k H H H h
B	1	M M.k k k H H H
B	10	M M M.k k k H H
B	100	G M M M.k k k H
B	1000	- G M M M.k k k

h = 0.1 Hz M = MHz
H = Hz G = GHz
k = kHz - = suppressed zero

6. Apply a 1 MHz 1 Vrms clock to the Rear Panel 1 MHz IN BNC connector. Select A INPUT-X1 and RESOLUTION Hz -1000 verify a display readout of 0. kHz and note that the GATE LED indicator flashes.

7. Press and latch the HOLD pushbutton switch and verify that the GATE LED indicator extinguishes. Press and unlatch the HOLD pushbutton switch.

8. Press and hold the RESET pushbutton switch and verify that the GATE LED indicator extinguishes, release the RESET pushbutton switch and verify that the GATE LED resumes flashing.

5.5 IEEE-488 CONFIDENCE CHECK

1. Connect a Systron-Donner Model 3520 Instrumentation Controller, or any other IEEE-488 controller to the Rear Panel IEEE-488 INTERFACE connector (J6).

2. Program the internal ADDRESS switch (A3S1) to 1 1 1 1 1 and place the internal PROG/TALK ONLY switch into its TALK ONLY position. Verify that the ADDRESS 5 4 3 2 1 LED indicators and the TALK ONLY LED indicator illuminates.

3. Program the ADDRESS switch to 1 1 0 0 1 and place the PROG/TALK ONLY switch into its PROG position, verify that the ADDRESS 4, 5 and 1 LED indicators illuminate and the ADDRESS 3 and 2 and the TALK ONLY indicators are extinguished. The preceeding internal ADDRESS and PROG switch settings assigned an ASCII 9 as a listen address and an ASCII Y as a talk address, and allows the Counter to accept data.

4. Keystroke the following entries into the 3520 Instrumentation Controller:

BUS CLR
RETURN
BUS REM
RETURN
BUS ADD 11001

Verify that the REMOTE, and kHz LED indicators illuminate; the 8-digit display indicates 0.0000 kHz and the Counter is placed into its hold function.

5. Keystroke the following entries into the 3520 Instrumentation Controller and verify the indication and/or functional selection of the Model 604XA Counter. Follow each entry with RETURN.

BUS OUT RETURN	O	Reset
BUS OUT RETURN	N	Sample
BUS OUT RETURN	M	Recycle
BUS OUT RETURN	L	Hold
BUS OUT RETURN	K	B Input selected (kHz LED Indicator extinguishes, MHz LED indicator illuminates and the display indicates 0.000 MHz).
BUS OUT RETURN	J	A Input X100 selected (MHz LED indicator extinguishes, kHz LED indicator illuminates and the display indicates 0.0000 kHz).
BUS OUT RETURN	I	A Input X10 selected.
BUS OUT RETURN	H	A Input X1 selected.
BUS OUT (or F or E) RETURN	G	0.1 Hz resolution selected (display indicates 0.0000 kHz).
BUS OUT RETURN	D	1 Hz resolution selected (display indicates 0.000 kHz).
BUS OUT RETURN	C	10 Hz resolution selected (display indicates 0.00 kHz).
BUS OUT (or @) RETURN	A	1000 Hz resolution selected (display indicates 0. kHz).
BUS IN RETURN PRINT AS RETURN	AS	Places the Counter into the TALK Mode, Counter outputs measurement data on the bus in 15-byte, 7-bit format in byte serial, bit parallel sequence. (Refer to Table 5-2 for measurement data format.)

The following programming information is provided to allow performance of the IEEE-488 Confidence Check using a Controller other than the Systron-Donner 3520.

When the Counter is turned on, its "wake up" state is as follows:

1. Counter is placed in its "Monitor" mode.

2. The RESOLUTION is set to .1 Hz (ASCII G).

3. The A INPUT X10 is selected (ASCII I).

4. The HOLD control function is selected (ASCII L).

Device dependent data can be programmed into the Remote Mode and addressed to listen. To place the Counter into Remote the assigned listen address (MLA) is entered while the REN is active. The Counter may also be placed into Remote by an ASCII @ through K entry.

The data is entered in serial bytes, consisting of 7-parallel bits. These data bytes may be entered in any order and need not be sequential. Table 5-3 provides the program Format for the Model 604XA Counter.

5.5 A INPUT PERFORMANCE TEST AND ADJUSTMENT PROCEDURE (All Models)

1. Select A INPUT ATTENUATION X1 and RESOLUTION Hz 1000.

2. Apply a 100 MHz signal at -5 dbm to the A INPUT connector.

3. Adjust A2R59 (BAL) while slowly decreasing the level of the 100 MHz input signal.

TABLE 5-2 OUTPUT DATA FORMAT

BYTE	BIT 7	6	5	4	3	2	1	ASCII CHARACTER	DATA FUNCTION
1	0	1	0	0	0	0	0	SP	NOT OFFSCALE
1	1	0	0	1	1	1	1	O	OFFSCALE
2	0	1	0	0	0	0	0	SP	NOT OFFSCALE
2	1	0	1	0	0	1	1	S	OFFSCALE
3	0	1	1	X	X	X	X	0→9	10^7 MSD
4	0	1	1	X	X	X	X	0→9	10^6
5	0	1	1	X	X	X	X	0→9	10^5
6	0	1	1	X	X	X	X	0→9	10^4
7	0	1	1	X	X	X	X	0→9	10^3
8	0	1	1	X	X	X	X	0→9	10^2
9	0	1	1	X	X	X	X	0→9	10^1
10	0	1	1	X	X	X	X	0→9	10^0 LSD
11	1	0	0	0	1	0	1	E	Exponent Pointer
12	0	1	0	1	0	1	1	+	Exponent Sign
12	0	1	0	1	1	0	1	—	Exponent Sign
13	0	1	1	X	X	X	X	0→3	Exponent Value
14	0	0	0	1	1	0	1	CR	Delimiter
15	0	0	0	1	0	1	0	LF	Delimiter

TABLE 5-3 MODEL 604XA PROGRAM FORMAT

BYTE	PROGRAM BITS 7	6	5	4	3	2	1	ASCII CHARACTER	FUNCTION
1	1	0	0	0	0	0	0	@	1 kHz RESOLUTION
	1	0	0	0	0	0	1	A	1 kHz RESOLUTION
	1	0	0	0	0	1	0	B	100 Hz RESOLUTION
	1	0	0	0	0	1	1	C	10 Hz RESOLUTION
	1	0	0	0	1	0	0	D	1 Hz RESOLUTION
	1	0	0	0	1	0	1	E	.1 Hz RESOLUTION
	1	0	0	0	1	1	0	F	.1 Hz RESOLUTION
	*1	0	0	0	1	1	1	G	.1 Hz RESOLUTION
2	1	0	0	1	0	0	0	H	A INPUT X1
	*1	0	0	1	0	0	1	I	A INPUT X10
	1	0	0	1	0	1	0	J	A INPUT X100
	1	0	0	1	0	1	1	K	B INPUT
3	*1	0	0	1	1	0	0	L	HOLD
	1	0	0	1	1	0	1	M	RECYCLE
4	1	0	0	1	1	1	0	N	SAMPLE
	1	0	0	1	1	1	1	O	RESET

*Wake-Up State

4. Verify the following sensitivity specifications:

20 Hz to 1 MHz -20 dBm (25 mV rms)
1 MHz to 5 MHz -13 dBm (50 mV rms)
5 MHz to 100 MHz -7 dBm (100 mV rms)

5. Check the operation of the A INPUT counter function from 20 Hz to 100 MHz at applied signal levels of 100 mV rms to its overload without damage levels (100 Vrms).

NOTE

Do not exceed an input level of 250 Vrms below 10 kHz, 50 Vrms from 10 kHz to 2 MHz and 5 Vrms from 2 MHz to 100 MHz.

5.6 MODEL 6042A B INPUT PERFORMANCE TEST AND ADJUSTMENT PROCEDURE

1. Select B INPUT and RESOLUTION Hz 1000.

2. Apply a 90 MHz to 520 MHz swept signal at -18 dBm to the B INPUT connector. Rotate A1R19 (SEN) fully CCW.

3. Manually adjust the Sweeper frequency and note the frequency that provides the least sensitivity (last negative deflection on Scope) at test point A1TP1.

4. Apply the frequency of least sensitivity (as noted in step 3) at a -20 dBm level and note the voltage at test point A1TP1.

5. Verify proper counter operation from 90 MHz to 520 MHz while adjusting the applied signal level to keep A1TP1 voltage at the level noted in step 4.

6. Apply the frequency of least sensitivity (as noted in step 3) at a -19 dBm level, and adjust potentiometer A1R19 (SEN) until the Counter just stops counting.

7. Apply a 100 to 512 MHz sweep frequency signal, while varying its level from -18 dBm to +20 dBm, and verify proper counter operation for all frequencies and input levels.

NOTE

If +27 dBm (5 Vrms) input signal level is exceeded, a .275A fuse located within the B INPUT connector will blow. Five spare input fuses are furnished with each counter.

5.7 MODEL 6043A B INPUT PERFORMANCE TEST AND ADJUSTMENT PROCEDURE

1. Select B INPUT and RESOLUTION Hz 1000.

2. Apply a 90 Hz to 1260 MHz sweep signal at -18 dBm to the B INPUT connector. Rotate A1R22 (SEN) fully CCW.

3. Adjust trimmer capacitors A1C5 and A1C16 for flatest response measured at test point A1TP1.

4. Adjust A1R15 (6.8V ADJ) for 6.8 Vdc as measured between pins 7 and 14 of IC A1U1.

5. Manually adjust the sweeper frequency and note the frequency that provides the least sensitivity at test point A1TP1.

6. Apply the frequency of least sensitivity noted in step 5 at a -20 dBm level and note the voltage at test point A1TP1.

7. Verify proper counter operation from 100 MHz to 1.25 GHz while adjusting the applied signal level to keep test point A1TP1 voltage at the level noted in step 6.

8. Apply the frequency of least sensitivity at -19 dBm level, and adjust potentiometer A1R22 (SEN) until the counter just stops counting.

9. Apply a 100 to 1250 MHz sweep frequency signal, while varying its level from -18 dBm to +20 dBm, and

verify proper counter operation for all frequencies and input levels.

NOTE

If +27 dBm (5 Vrms) input signal level is exceeded, a .275A fuse located within the B INPUT connector will blow. Five spare input fuses are furnished with each counter.

5.8 INTEGRATED CIRCUIT DATA

The major IC components in the 604XA series Frequency Counters are described in this section to aid troubleshooting and repair of the unit. Components are not described in complete detail, but are extracts from the manufacturers specification catalog. For those IC's not described or if more significant characteristics are required, refer to the appropriate manufacturers specification sheet and/or catalog. Table 5-4 lists the IC's in alphanumeric order by base number.

TABLE 5-4 I.C. COMPONENT DESCRIPTION

COMPONENT NUMBER	TITLE	S-D PART NUMBER	PAGE
055095	6-Digit Counter	055095	5-9
MC10100P	Quad 2-Input NOR with Strobe	103712	5-11
MC10115L	Quad Line Receiver	045254	5-12
MC10124L	Quad TTL to ECL Translator	045228	5-13
MC10125L	Quad ECL to TTL Translator	045226	5-14
MC10131L	Dual D Master-Slave Flip Flop	045239	5-15
MC10138P	ECL Bi-Quinary Counter	103837	5-16
MC14013BCP	Dual D F/F	103199	5-17
MC14050BP	Noninverting Hex Buffer	103492	5-18
MC14512BCP	8-Channel Data Selector	103942	5-19
MC14518BCP	Dual BCD Up Counter	103339	5-20
MC14528BCP	Dual Monostable Multivibrator	045289	5-21
MC14532BCP	8-Bit Priority Encoder	116213	5-22
MC3446	Quad Interface Bus Transceiver	117021	5-23
CD4049	Hex Inverting Buffer	103217	5-24
NE555V	Timer	045208	5-25
SN72311P	Differential Comparator with Strobe	103943	5-26
SN74LS00N	Quad 2-Input NAND	103130	5-27
SN74LS04N	Hex Inverter	103749	5-28
SN74LS08N	Quad 2-Input AND	103967	5-29
SN74LS10N	Triple 3-Input NAND	103968	5-29
SN74LS123N	Dual Retriggerable Monostable MV with Clear	103976	5-30
SN74LS145N	BCD-to-Decimal Decoder/Driver	103369	5-31
SN74LS157N	Quad 2 to 1 Data Selector/Multiplexer	117249	5-31
SN74LS196N	Presettable Decade Counter	103164	5-32
SN74LS197N	Presetable Binary Counter	103165	5-33
SN74LS20N	Dual 4-Input Positive NAND	103969	5-34
SN74LS30N	8-Input NAND	103971	5-35
SN74LS32N	Quad 2-Input OR	103972	5-29
SN74LS74N	Dual D Flip Flop with Preset and Clear	103132	5-30
SN7416N	Hex Inverter Buffer/Driver	045230	5-36
SN74188N	32 x 8 Programmable ROM	055998	5-37
SN74247N	BCD to 7-Segment Decoder/Driver	103314	5-38
SN7426N	Quad 2-Input NAND	045252	5-35
SN7489N	16 x 4 Read/Write Memory	103219	5-27
SN75451AP	Dual and Peripheral Drivers	045290	5-40
MC7805CT	3-Terminal Positive Voltage Regulator	045256	5-41
MC7902CT	3-Terminal Negative Voltage Regulator	103944	5-42
MC7905.2CP	3-Terminal Negative Voltage Regulator	103033	5-43
SP8617B	Divide by 4 Prescaler	117476	
93L24PC	5-Bit Comparator	117020	5-44

SD055095 S-D P/N 055095

The circuitry of this 40 pin CMOS Decade Count Chain contains; a six decade divider chain, an over-flow detector, 33-Bit Storage register, a multiplex, an adjustable multiplex free-running M.V. clock, a blank code generator/decimal point activator, and a clock selector allowing for the provision to break the decade chain into two chains of three decades each.

Listed by pin number are the inputs and outputs of the device, with signal name and functional details.

Pin No.	Signal Name	Function
1	TEST CLOCK ENABLE	Allows the three MSD of the decade chain to be driven by the TEST CLOCK when set high.
2	TEST CLOCK	Clock input to the 3rd MSD of the count chain, enabled when the TEST CLOCK ENABLE is set high.
3	LSD 8	LSD Bit "8" input.
4	LSD 4	LSD Bit "4" input.
5	LSD 2	LSD Bit "2" input.
6	LSD 1	LSD Bit "1" input.
7	DECADE CLOCK	Clock input to the LSD decade of the count chain.
8	Not Used	
9	Not Used	
10	SLSD 8	NLSD Bit "8" input.
11	SLSD 4	NLSD Bit "4" input.
12	SLSD 2	NLSD Bit "2" input.
13	SLSD 1	NLSD Bit "1" input.
14	Not Used	
15	Vcc	+ voltage supply input +4.5 to +5.5 Vdc ⩽50 mV p-p ripple or noise.
16	BCD1	Multiplexed BCD Bit "1" output.
17	BCD2	Multiplexed BCD Bit "2" output.
18	SUPPLEMENTAL OUTPUT	Carry from the NMSD of the count chain.
19	BCD 4	Multiplexed BCD Bit "4" output.
20	BCD 8	Multiplexed BCD Bit "8" output.
21	BLANK CODE	Indicates that the LSD was present on the BCD output pins. The BLANK CODE will reset (go to logic high) on the detection of the first of the following three conditions; 1) Detection of an Over Flow. 2) Detection of a logic high on any of the BCD outputs. 3) Detection of a coincidence of any of the

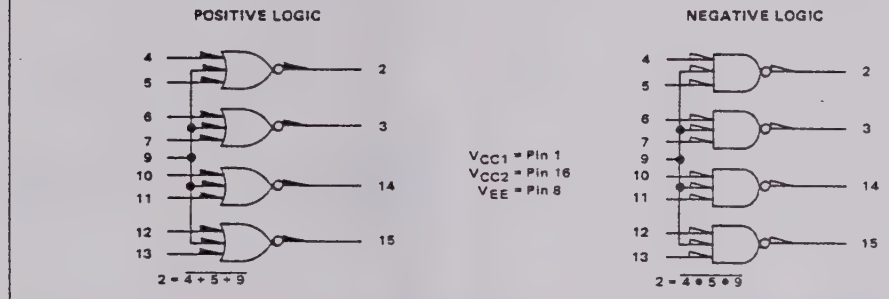
Pin No.	Signal Name	Function
21	BLANK CODE (Cont)	position and Octal Code listed as follows: Position — Octal Code 1 — 7 2 — 6 3 — 5 4 — 4 5 — 3 6 — 2 7 — 1 8 — 0
22	DECIMAL POINT	A decimal point actuation when position output coincides with the proper octal code input.
23 24 25	OCTAL CODE BIT 4 OCTAL CODE BIT 2 OCTAL CODE BIT 1	The octal code inputs can be considered as static logic levels, they may be changed at any time, but will not effect outputs until the completion of a full multiplexer cycle.
26	OVER FLOW	Indicates that the MSD of the count chain has generated a carry. This function must be reset by a Master Reset on pin 40, to return to its logic low state.
27	STORE	True (Active) level 0 to +5 Vdc. False level +2.5 Vdc to Vcc. Requires a pulse duration of ≥ 1 μs. When placed at a static true (logic low) the 33 storage registers will follow their data inputs.
28	MULTIPLEX RATE CONTROL	When connected to an external timing capacitor, it will allow the multiplexer M.V. to free-run between 2 kHz to 32 kHz, depending on the value of the capacitor. When connected to an external clock it will allow triggering of the M.V. (2 kHz to 32 kHz).
29	PT/NT	When placed at ground it configures the position outputs to 0 volts true (negative transistion). When left open or pulled up to Vcc configures the position outputs to Vcc true (position transistion).
30 31 32 33 34 35 36 37 38	POS1 POS2 POS4 POS3 POS6 Not Used POS5 POS8 POS7	Position outputs are negative true when pin 29 is at ground, and positive true when pin 29 is left open or pulled up to Vcc.
39	GND	Provides the ground return for the Vcc supply.
40	RESET	Will reset the six decade counters of the count chain and the over-flow detector, when placed at a logic low (0 Vdc to +0.5 Vdc) for a duration of ≥ 1 μs.

ECL QUAD 2-INPUT NOR GATE WITH STROBE

MC10100 S-D P/N 103712

The MC10100 is a quad NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates. Input pulldown resistors eliminate the need to tie unused inputs to a voltage supply. Open emitter outputs permit wire-ORing and direct connection to busses.

P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ

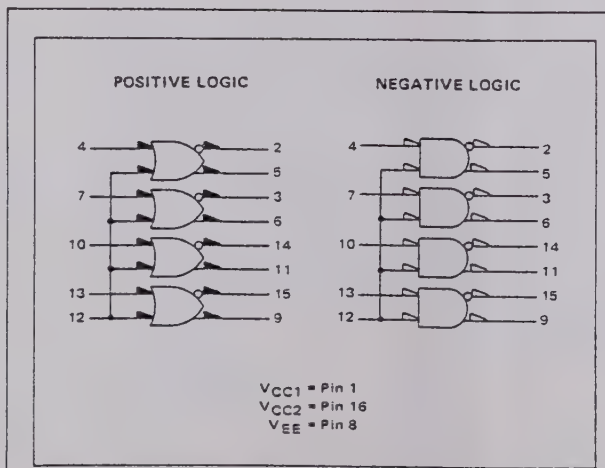


ECL QUAD OR/NOR GATE

MC10101 S-D P/N 025791

The MC10101 is a quad 2-input OR/NOR gate with one input from each gate common to pin 12. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

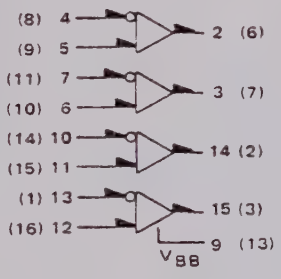
P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
Output Rise and Fall Time:
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)



MC10115L

S-D P/N 045254

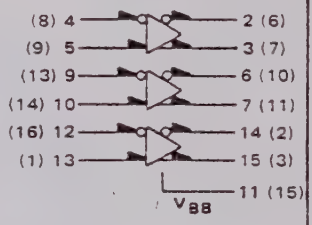
MC10115/MC10515



These receivers are designed for use in sensing differential signals over long lines. The bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide these receivers with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent upsetting the current source bias network.

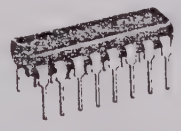
MC10116/MC10516



t_{pd} = 2.0 ns typ
P_D = 110 mW typ/pkg (No Load)

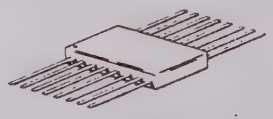
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

t_{pd} = 2.0 ns typ
P_D = 85 mW typ/pkg (No Load)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10115 and
MC10116 only

L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10515 and
MC10516 only

Numbers at ends of terminals denote pin numbers for L and P package
Numbers in parenthesis denote pin numbers for F package

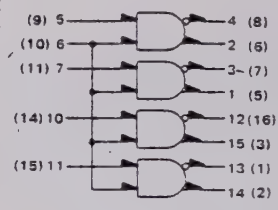
One input from each gate must be tied to V_{BB} during testing.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E											mAdc
MC10115/10515		–	29	–	29	–	26	–	29	–	29	
MC10116/10516		–	24	–	23	–	21	–	23	–	24	
Input Current	I_{inH}	–	165	–	150	–	95	–	95	–	95	µAdc
	I_{CBO}	–	1.5	–	1.5	–	1.0	–	1.0	–	1.0	µAdc
Reference Voltage	V_{BB}	-1.440	-1.320	-1.420	-1.280	-1.350	-1.230	-1.295	-1.150	-1.240	-1.120	Vdc
Switching Times												ns
Propagation Delay	t_{pd}	1.0	3.5	1.0	3.1	1.0	2.9	1.0	3.3	1.0	4.0	
Rise Time, Fall Time (20% to 80%)	t_+, t_-	1.0	3.9	1.1	3.6	1.1	3.3	1.1	3.7	1.0	4.4	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10124L

S-D P/N 045228



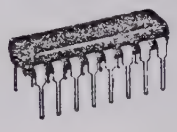
Gnd = Pin 16 (4)
V_{CC} (+5.0 Vdc) = Pin 9 (13)
V_{EE} (−5.2 Vdc) = Pin 8 (12)
$V_{CC}max$ = 7.0 Vdc

P_D = 380 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ (+1.5 Vdc in to 50% out)
t+, t− = 2.5 ns typ (20% to 80%)

The MC10124/MC10524 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The device has TTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

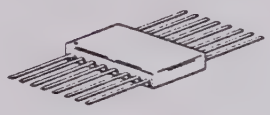
Power supply requirements are ground, +5.0 Volts, and −5.2 Volts. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by any of the MECL line receivers or the MC10125 MECL to TTL translator or the MC10177 MECL to MOS translator.



P SUFFIX
CERAMIC PACKAGE
CASE 648
MC10124 only

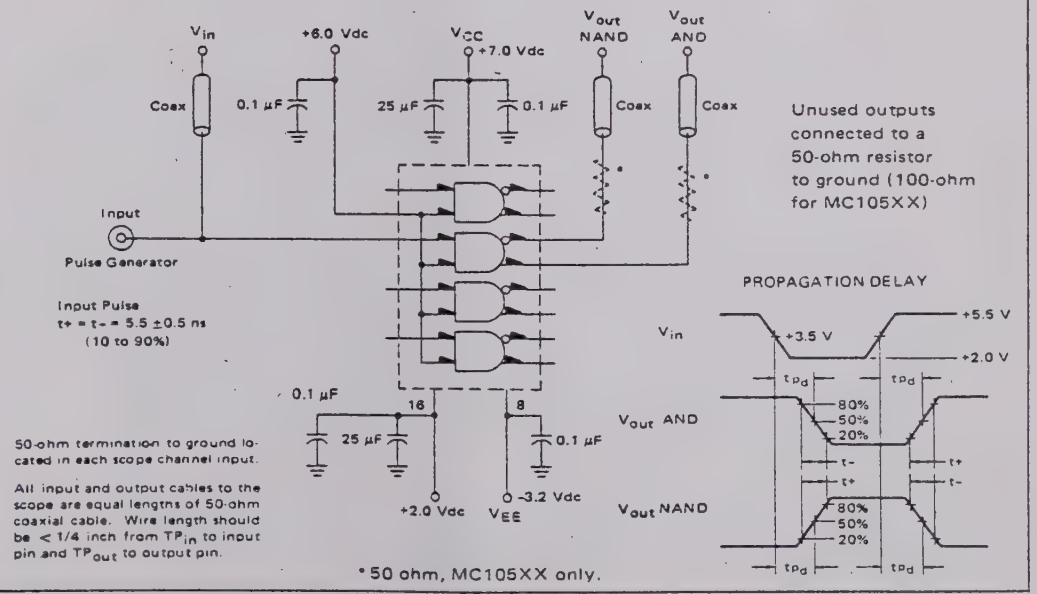
L SUFFIX
CERAMIC PACKAGE
CASE 620



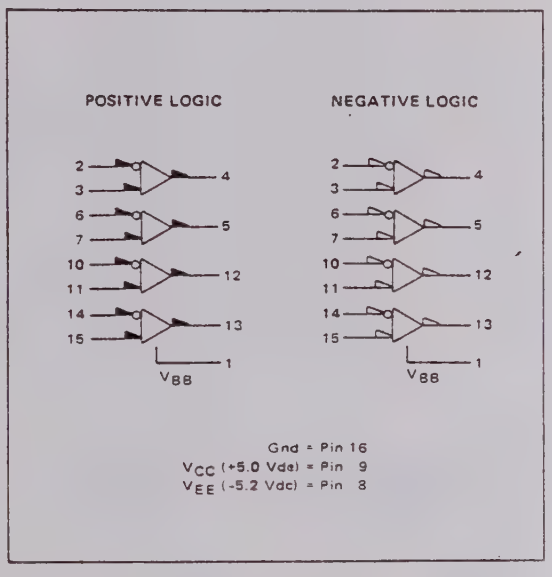
F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10524 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE: All power supply and logic levels are shown shifted 2 volts positive.



The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky MTTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on pin 1 for use in Schmitt trigger applications and single-ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and -5.2 Volts. Propagation delay of the MC10125 is typically 5.0 ns. The MC10125 has fanout of 10 MTTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or MTTL out. This device has an input common mode noise rejection of ±1.0 Volt.

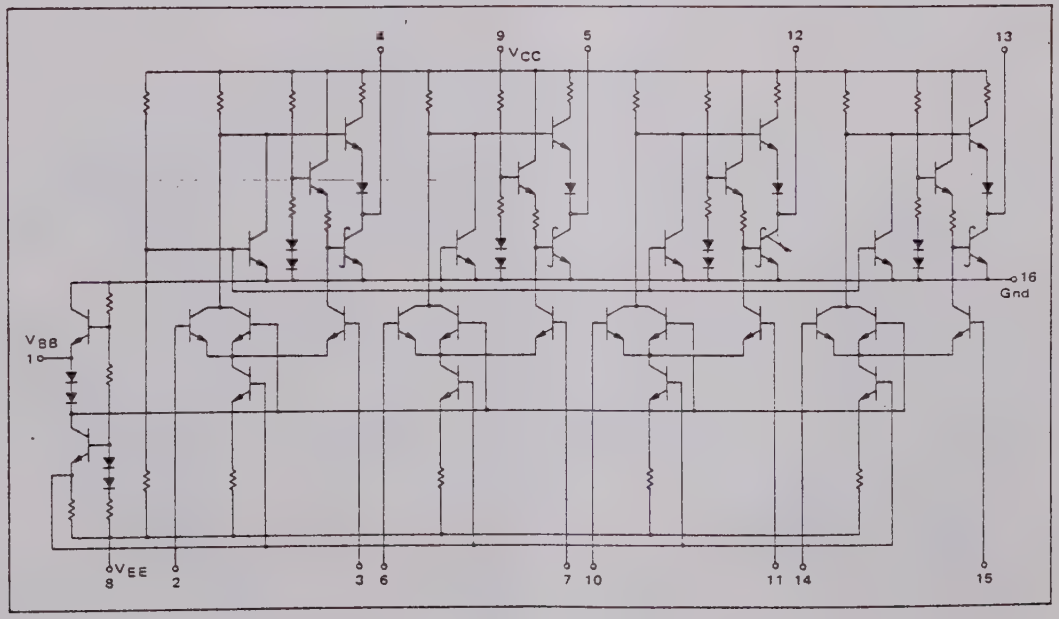
An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the MTTL equipment. This isolates the MECL logic from the noisy MTTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

P_D = 380 mW typ/pkg (No Load)

t_{pd} = 4.5 ns typ (50% to +1.5 Vdc out)

Output Rise, Fall Times:
2.5 ns typ (20% to 80%)

CIRCUIT SCHEMATIC



R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

ϕ = Don't Care

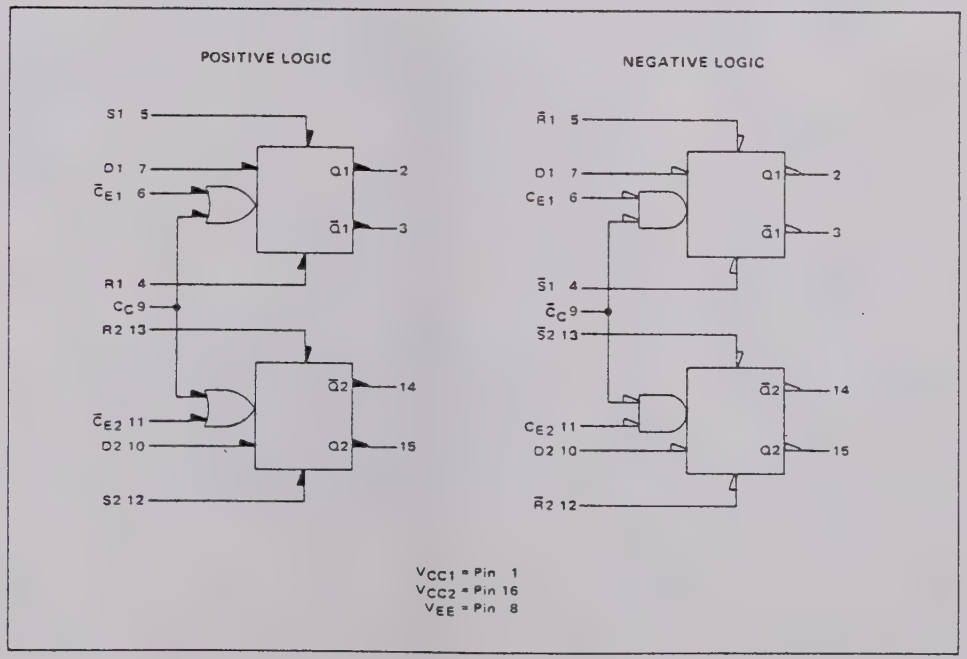
$C = \overline{C}_E + C_C$

A clock H is a clock transition from a low to a high state.

The MC10131 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{C}_E$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}. Output rise and fall times have been optimized to provide relaxation of system design and layout criteria.

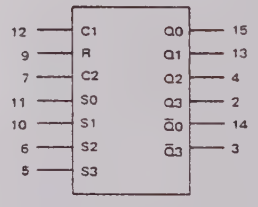


The MC10138 is a four bit counter capable of divide by two, five, or ten functions. It is composed of four set-reset master-slave flip-flops. Clock inputs trigger on the positive going edge of the clock pulse.

Set or reset input override the clock, allowing asynchronous "set" or "clear". Individual set and common reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

P_D = 370 mW typ/pkg (No Load)
f_{tog} = 150 MHz typ

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8



COUNTER TRUTH TABLES

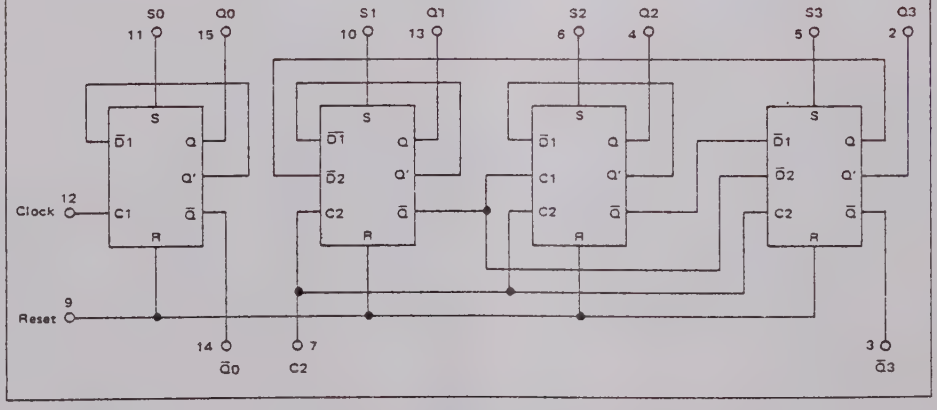
BI-QUINARY
(Clock connected to C2 and Q3 connected to C1)

COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	H	H
6	H	L	H	H
7	L	L	H	H
8	H	H	L	H
9	L	H	L	H

BCD
(Clock connected to C1 and Q0 connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

BLOCK DIAGRAM



604XA-2-80

DUAL TYPE D FLIP-FLOP

The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Toggle Rate = 4 MHz typical @ 5 Vdc
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL TYPE D FLIP-FLOP

L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

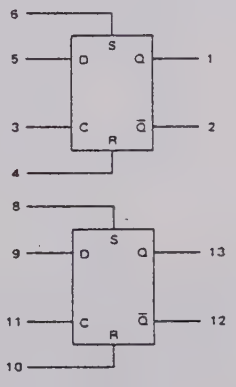
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS				OUTPUTS		
CLOCK†	DATA	RESET	SET	Q	$\overline{Q}$	
⌐⌐	0	0	0	0	1	
⌐⌐	1	0	0	1	0	
⌐⌐	X	0	0	Q	$\overline{Q}$	No Change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = Don't Care
† = Level Change

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

MC14049
MC14050

S-D P/N 103217
S-D P/N 103492

HEX BUFFERS

The MC14049UB hex inverter/buffer and MC140508 noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{CC}. The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage for logic-level conversions. Two TTL/DTL Loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (V_{CC} = 5.0 V, $V_{OL} \leq 0.4$ V, $I_{OL} \geq 3.2$ mA). Note that pin 16 is not connected internally on these devices; consequently connections to this terminal will not affect circuit operation.

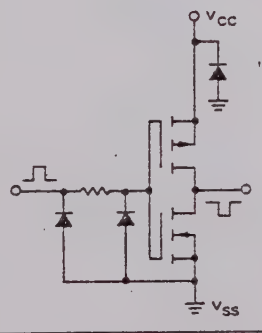
- High Source and Sink Currents
- High-to-Low Level Converter
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Meets JEDEC UB Specifications—MC14049UB
  Meets JEDEC B Specification—MC14050B

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

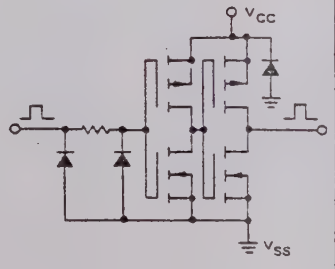
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to +18	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	45	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)

MC14049UB



MC140508

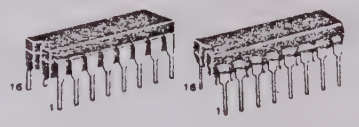


CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX BUFFERS

Inverting — MC14049UB
Noninverting — MC14050B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

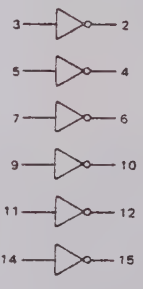
ORDERING INFORMATION

MC14XXXUB
MC14XXXB

Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

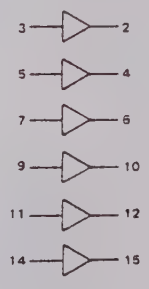
LOGIC DIAGRAMS

MC14049UB



NC = Pin 13, 16
V_{SS} = Pin 8
V_{CC} = Pin 1

MC14050B



NC = Pin 13, 16
V_{SS} = Pin 8
V_{CC} = Pin 1

8-CHANNEL DATA SELECTOR

The MC14512B is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- High Fanout > 50
- Single Supply Operation — Positive or Negative
- 3-State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-CHANNEL DATA SELECTOR

L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

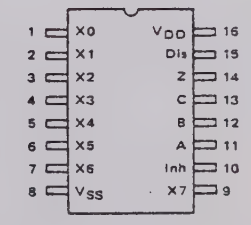
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
φ	φ	φ	1	0	0
φ	φ	φ	φ	1	High Impedance

φ = Don't Care

PIN ASSIGNMENT

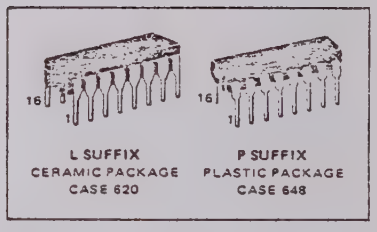


This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

DUAL UP COUNTERS

The MC14518 dual BCD counter and the MC14520 dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-floos, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518 will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

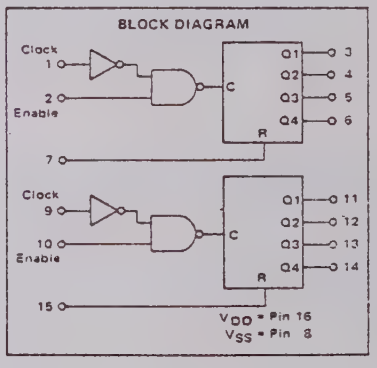
DUAL BCD UP COUNTER
(MC14518)
DUAL BINARY UP COUNTER
(MC14520)



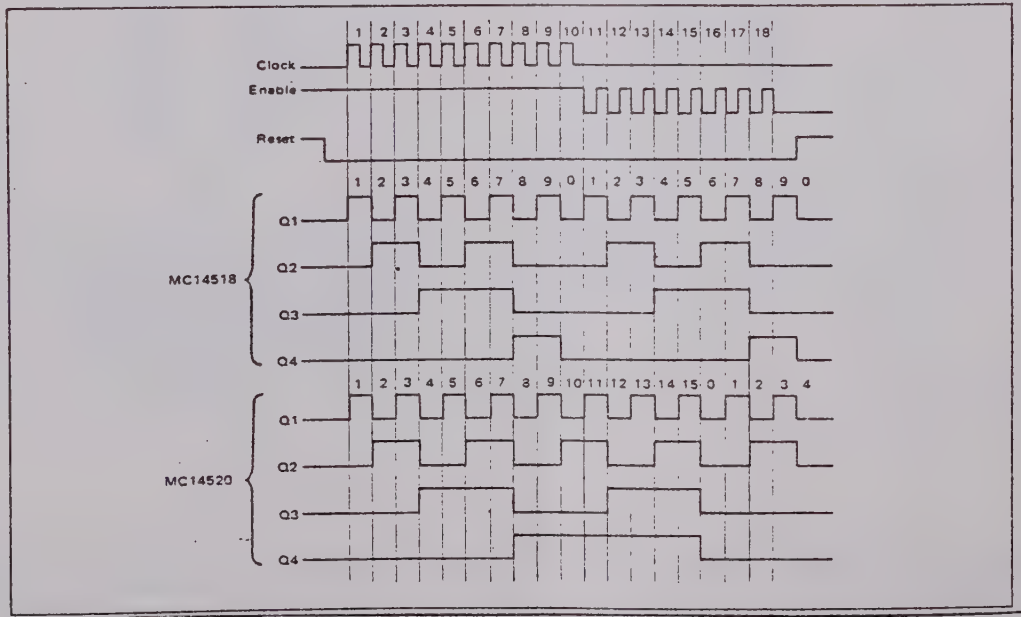
TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
⌐	1	0	Increment Counter
0	⌐	0	Increment Counter
⌐	X	0	No Change
X	⌐	0	No Change
⌐	0	0	No Change
1	⌐	0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care



TIMING DIAGRAM



DUAL MONOSTABLE MULTIVIBRATOR

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

- Separate Reset Available
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- See MC14538B Data Sheet for Applications Requiring Precise Control of Output Pulse Width

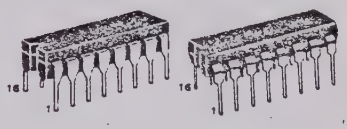
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR



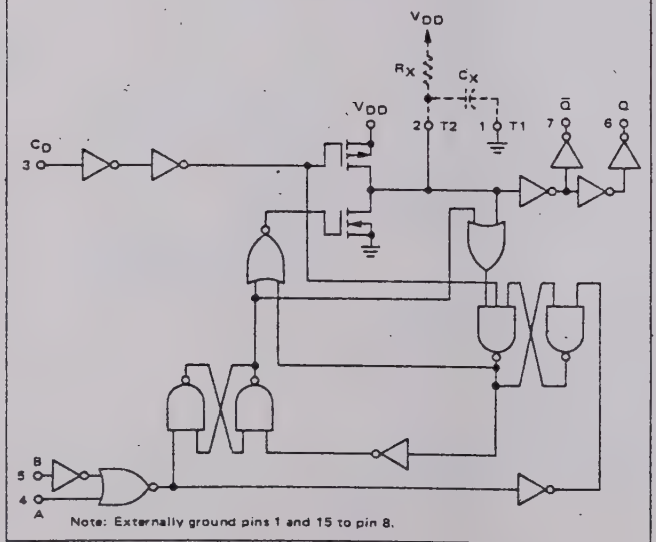
L SUFFIX CERAMIC PACKAGE CASE 620

P SUFFIX PLASTIC PACKAGE CASE 648

ORDERING INFORMATION

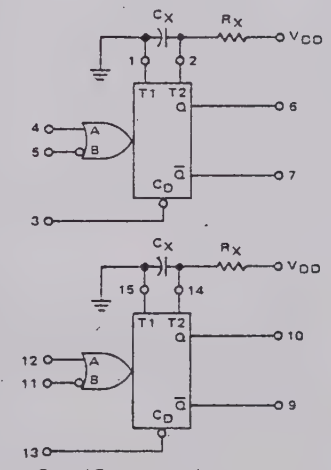
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

LOGIC DIAGRAM
(1/2 of Device Shown)



Note: Externally ground pins 1 and 15 to pin 8.

BLOCK DIAGRAM



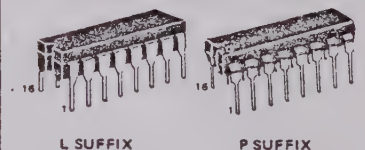
RX and CX are external components.

VDD = Pin 16
VSS = Pin 8

8-BIT PRIORITY ENCODER

The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (E_{in}) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E_{out}).

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Low Input Capacitance — 5.0 pF typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

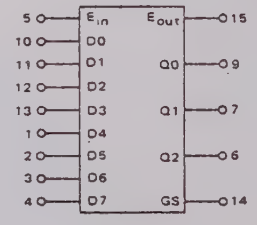
TRUTH TABLE

INPUT									OUTPUT				
E_{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

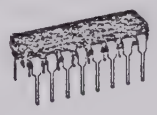
MC3446A S-D P/N 11702!

QUAD GENERAL-PURPOSE INTERFACE BUS (GPIB) TRANSCEIVER

The MC3446A is a quad bus transceiver intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. This transceiver allows the bidirectional flow of digital data and commands between the various instruments. The transceiver provides four open-collector drivers and four receivers featuring hysteresis.

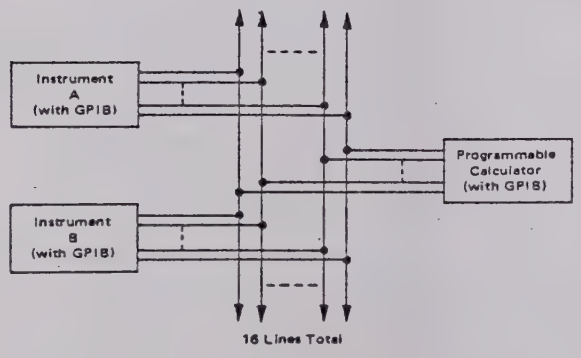
- Tailored to Meet the IEEE Standard 488-1978 (Digital Interface for Programmable Instrumentation) and the Proposed IEC Standard on Instrument Interface
- Provides Electrical Compatibility with General-Purpose Interface Bus (GPIB)
- MOS Compatible with High Impedance Inputs
- Driver Output Guaranteed Off During Power Up/Power Down
- Low Power — Average Power Supply Current = 12 mA
- Terminations Provided

QUAD INTERFACE BUS TRANSCEIVER
SILICON MONOLITHIC INTEGRATED CIRCUIT

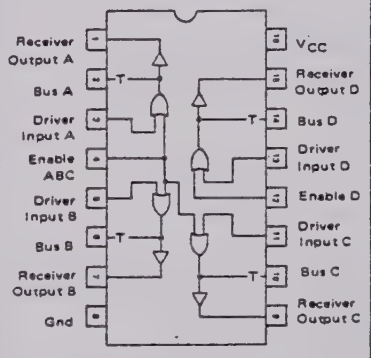


P SUFFIX
PLASTIC PACKAGE
CASE 648

TYPICAL MEASUREMENT SYSTEM APPLICATION



PIN CONNECTIONS



— T — = Bus Termination

COS/MOS Hex Buffer/Converters

CD4049A—Inverting Type
CD4050A—Non-Inverting Type

The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, V_{OL} ≥0.4 V, and I_{DN} ≥3.2 mA.)

The CD4049A and CD4050A are designated as replacements for CD4009A and CD4010A, respectively. Because the CD4049A and CD4050A require only one power supply, they are preferred over the CD4009A and CD4010A and should be used in place of the CD4009A and CD4010A in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049A and CD4050A are pin compatible with the CD4009A and CD4010A respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049A or CD4050A, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069 Hex Inverter is recommended.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:
- High sink current for driving 2 TTL loads
- High-to-low level logic conversion
- Quiescent current specified to 15 V
- Maximum input leakage of 1 μA at 15 V (full package-temperature range)

Applications:
- COS/MOS to DTL/TTL hex converter
- COS/MOS current "sink" or "source" driver
- COS/MOS high-to-low logic-level converter

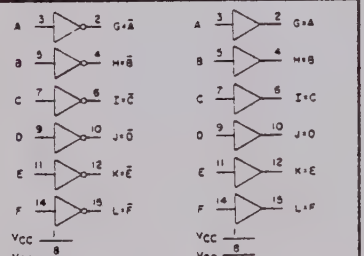


Fig. 1 – Functional diagrams.

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (V_{CC}) (For T_A=Full Package-Temperature Range)	3	12	V
Input Voltage Range (V_I)	V_{CC}*	12	V

*The CD4049 and CD4050 have high-to-low-level voltage conversion capability but not low-to-high-level, therefore it is recommended that $V_I \geq V_{CC}$

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	Conditions V_{IN} (V)	Conditions V_{CC} (V)	Limits at Indicated Temperatures (°C) *D,K,F,H Packages* −55	+25 Typ.	+25 Limit	+125	*E Package* −40	+25 Typ.	+25 Limit	+85	Units
Quiescent Device Current, I_L Max.	–	–	5	0.3	0.01	0.3	20	3	0.03	3	42	μA
	–	–	10	0.5	0.01	0.5	30	5	0.05	5	70	
	–	–	15	10	0.02	10	100	50	0.05	50	500	
Output Voltage: Low-Level, V_{OL}	–	0, 5	5	0 Typ.; 0.05 Max.								V
	–	0, 10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0, 5	5	4.95 Min.; 5 Typ.								
	–	0, 10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL} CD4050A	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH} All Types	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Inputs Low, V_{NL} CD4049A	3.6	–	5	1 Min.; 1.5 Typ.								
	7.2	–	10	2 Min.; 3 Typ.								
Noise Margin: Inputs Low, V_{NML} Min. CD4050A	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH} Min. CD4050A	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_{DN} Min.	0.4	–	4.5	3.3	5.2	2.6	1.8	3.1	5.2	2.6	2.1	mA
	0.4	–	5	3.75	6	3	2.1	3.6	6	3	2.5	
	0.5	–	10	10	16	8	5.6	9.6	16	8	6.6	
P-Channel (Source), I_{DP} Min.	4.5	–	5	−0.62	−1	−0.5	−0.35	−0.6	−1	−0.5	−0.4	
	2.5	–	5	−1.85	−2.5	−1.25	−0.9	−1.5	−2.5	−1.25	−1	
	9.5	–	10	−1.85	−2.5	−1.25	−0.9	−1.5	−2.5	−1.25	−1	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

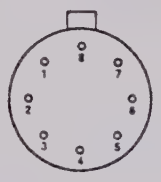
NE555V

S-D P/N 045208

DESCRIPTION

The NE/SE 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA or drive TTL circuits.

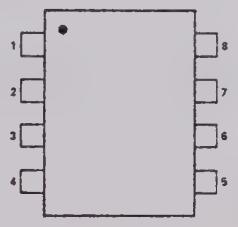
PIN CONFIGURATIONS



T PACKAGE
(Top View)

1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDER PART NOS. SE555T/NE555T

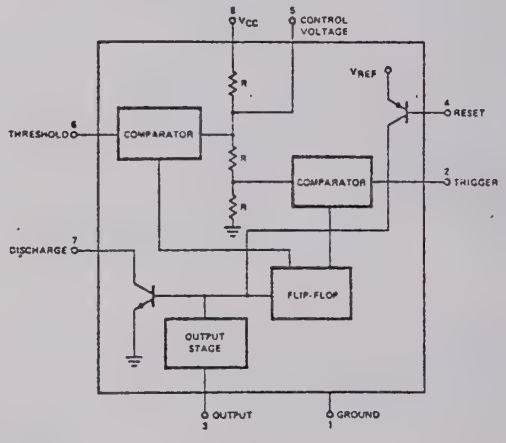


V PACKAGE
(Top View)

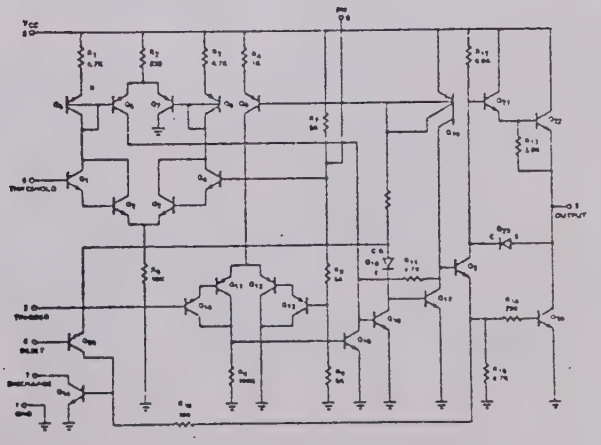
1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ORDER PART NOS. SE555V/NE555V

BLOCK DIAGRAM



EQUIVALENT CIRCUIT



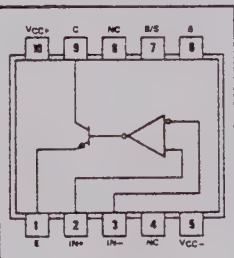
description

The SN52111 and SN72311 are single high-speed voltage comparators. These devices are designed to operate from a wide range of power supply voltage, including ±15-volt supplies for operational amplifiers and 5-volt supplies for logic systems. The output levels are compatible with most DTL, TTL, and MOS circuits. These comparators are capable of driving lamps or relays and switching voltages up to 50 volts at 50 milliamperes. All inputs and outputs can be isolated from system ground. The outputs can drive loads referenced to ground, V_{CC+}, or V_{CC-}. Offset balancing and strobe capability are available and the outputs can be wire-OR connected. If the strobe input is low, the output will be in the off state regardless of the differential input. Although slower than the SN52506 and SN52514, these devices are not as sensitive to spurious oscillations.

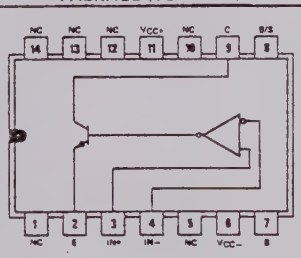
The SN52111 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN72311 is characterized for operation from 0°C to 70°C.

terminal assignments

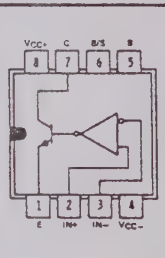
FA FLAT PACKAGE (TOP VIEW)



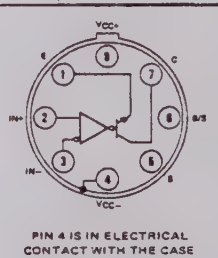
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



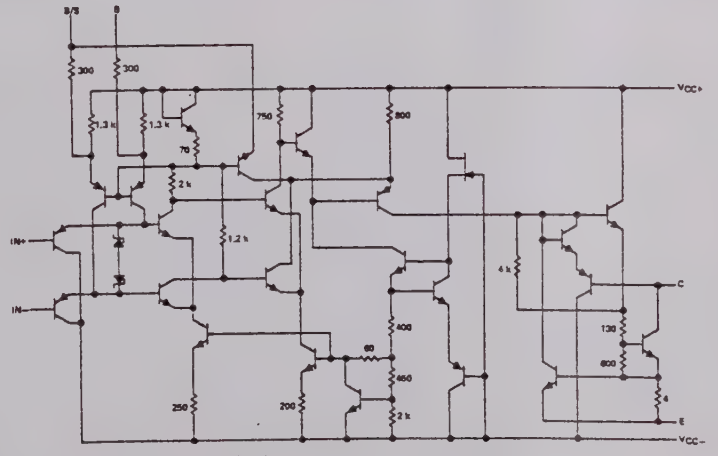
JP OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



L PLUG-IN PACKAGE (TOP VIEW)



schematic



B	Balance
B/S	Balance/Strobe
C	Collector Output
E	Emitter Output
IN+	Noninverting Input
IN−	Inverting Input
NC	No Internal Connection
V_{CC+}	Positive Supply Voltage
V_{CC-}	Negative Supply Voltage

Resistor values shown are nominal and in ohms.

64-BIT READ/WRITE MEMORIES

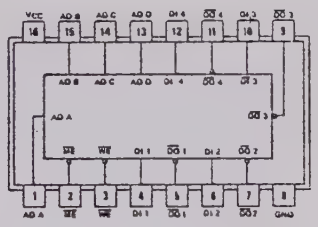
SN7489N

S-D P/N 103219

64-BIT READ/WRITE MEMORIES

89 16 4-BIT WORDS

See Bipolar Microcomputer Components Data Book, LCC4270



SN7489 (J, N)

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

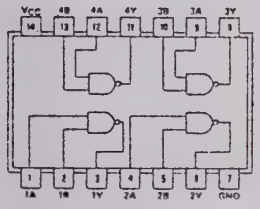
SN74LS00N

S-D P/N 103130

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

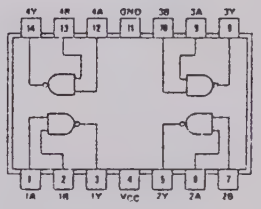
00

positive logic:
$Y = \overline{AB}$



SN5400 (J)
SN54H00 (J)
SN54L00 (J)
SN54LS00 (J, W)
SN54S00 (J, W)

SN7400 (J, N)
SN74H00 (J, N)
SN74L00 (J, N)
SN74LS00 (J, N)
SN74S00 (J, N)



SN5400 (W)
SN54H00 (W)
SN54L00 (T)

HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

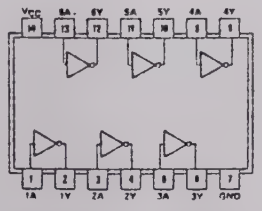
SN74LS05

S-D P/N 116113

HEX INVERTERS
WITH OPEN-COLLECTOR OUTPUTS

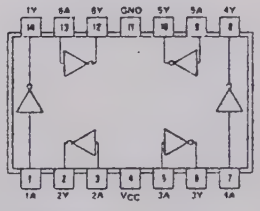
05

positive logic:
$Y = \overline{A}$



SN5405 (J)
SN54H05 (J)
SN54LS05 (J, W)
SN54S05 (J, W)

SN7405 (J, N)
SN74H05 (J, N)
SN74LS05 (J, N)
SN74S05 (J, N)



SN5405 (W)
SN54H05 (W)

SN74LS04N

S-D P/N 103749

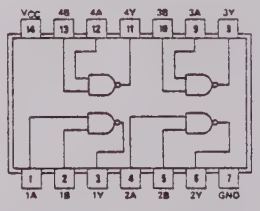
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

03

positive logic:
$Y = \overline{AB}$

See page 6-4



SN5403 (J)
SN54L03 (J)
SN54LS03 (J, W)
SN54S03 (J, W)

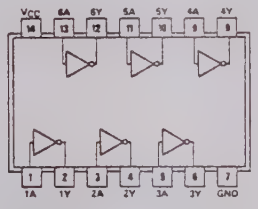
SN7403 (J, N)
SN74L03 (J, N)
SN74LS03 (J, N)
SN74S03 (J, N)

HEX INVERTERS

04

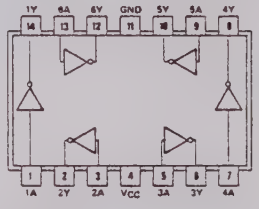
positive logic:
$Y = \overline{A}$

See page 6-2



SN5404 (J)
SN54H04 (J)
SN54L04 (J)
SN54LS04 (J, W)
SN54S04 (J, W)

SN7404 (J, N)
SN74H04 (J, N)
SN74L04 (J, N)
SN74LS04 (J, N)
SN74S04 (J, N)



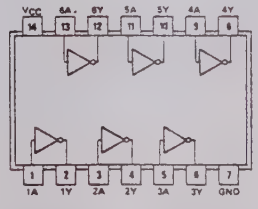
SN5404 (W)
SN54H04 (W)
SN54L04 (T)

HEX INVERTERS
WITH OPEN-COLLECTOR OUTPUTS

05

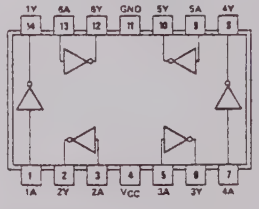
positive logic:
$Y = \overline{A}$

See page 6-4



SN5405 (J)
SN54H05 (J)
SN54LS05 (J, W)
SN54S05 (J, W)

SN7405 (J, N)
SN74H05 (J, N)
SN74LS05 (J, N)
SN74S05 (J, N)



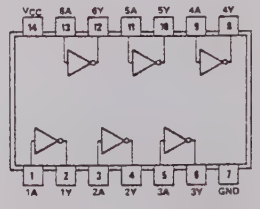
SN5405 (W)
SN54H05 (W)

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

06

positive logic:
$Y = \overline{A}$

See page 6-24



SN5406 (J, W)

SN7406 (J, N)

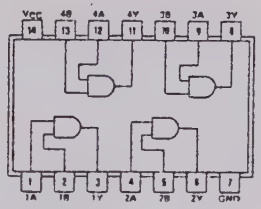
QUADRUPLE 2-INPUT POSITIVE-AND GATES

SN74LS08N — S-D P/N 103967

QUADRUPLE 2-INPUT
POSITIVE-AND GATES

08

positive logic:
$Y = AB$



SN5408 (J, W) SN7408 (J, N)
SN54LS08 (J, W) SN74LS08 (J, N)
SN54S08 (J, W) SN74S08 (J, N)

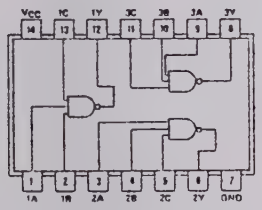
TRIPLE 3-INPUT POSITIVE-NAND GATES

SN74LS10N — S-D P/N 103968

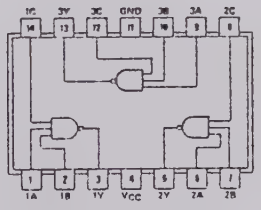
TRIPLE 3-INPUT
POSITIVE-NAND GATES

10

positive logic:
$Y = \overline{ABC}$



SN5410 (J) SN7410 (J, N)
SN54H10 (J) SN74H10 (J, N)
SN54L10 (J) SN74L10 (J, N)
SN54LS10 (J, W) SN74LS10 (J, N)
SN54S10 (J, W) SN74S10 (J, N)



SN5410 (W)
SN54H10 (W)
SN54L10 (T)

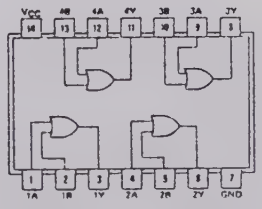
QUADRUPLE 2-INPUT POSITIVE-OR GATES

SN74LS32N — S-D P/N 103972

QUADRUPLE 2-INPUT
POSITIVE-OR GATES

32

positive logic:
$Y = A+B$



SN5432 (J, W) SN7432 (J, N)
SN54LS32 (J, W) SN74LS32 (J, N)
SN54S32 (J, W) SN74S32 (J, N)

4 LINE-TO-10-LINE DECODERS

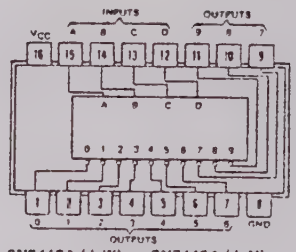
SN74LS42N S-D P/N 103131

4 LINE-TO-10-LINE DECODERS

42 BCD-TO-DECIMAL

43 EXCESS-3-TO-DECIMAL

44 EXCESS-3-GRAY-TO-DECIMAL



SN5442A (J, W) SN7442A (J, N)
SN54L42 (J) SN74L42 (J, N)
SN54LS42 (J, W) SN74LS42 (J, N)
SN5443A (J, W) SN7443A (J, N)
SN54L43 (J) SN74L43 (J, N)
SN5444A (J, W) SN7444A (J, N)
SN54L44 (J) SN74L44 (J, N)

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

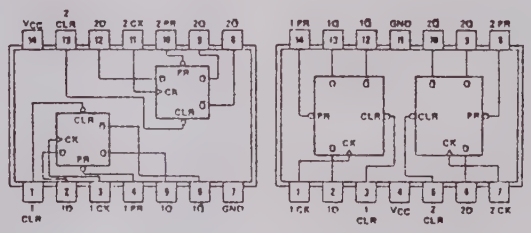
SN74LS74N S-D P/N 103132

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

74

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$



SN5474 (J) SN7474 (J, N) SN5474 (W)
SN54H74 (J) SN74H74 (J, N) SN54H74 (W)
SN54L74 (J) SN74L74 (J, N) SN54L74 (T)
SN54LS74A (J, W) SN74LS74A (J, N)
SN54S74 (J, W) SN74S74 (J, N)

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

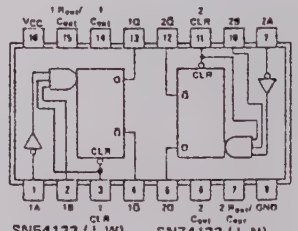
SN74LS123N S-D P/N 103976

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

123

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎



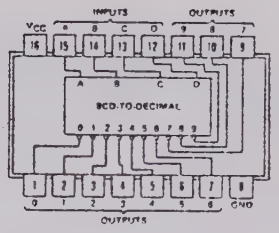
SN54123 (J, W) SN74123 (J, N)
SN54L123 (J) SN74L123 (J, N)
SN54LS123 (J, W) SN74LS123 (J, N)

BCD-TO-DECIMAL DECODERS/DRIVERS FOR LAMPS, RELAYS, MOS

SN74LS145N S-D P/N 103369

BCD-TO-DECIMAL DECODERS/DRIVERS FOR LAMPS, RELAYS, MOS

145 BCD-TO-DECIMAL



SN54145 (J, W) SN74145 (J, N)
SN54LS145 (J, W) SN74LS145 (J, W)

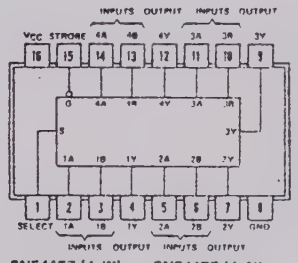
QUAD 2-TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SN74LS157 S-D P/N 117249

QUAD 2- TO 1-LINE DATA SELECTORS/MULTIPLEXERS

157 NONINVERTED DATA OUTPUTS

158 INVERTED DATA OUTPUTS



SN54157 (J, W) SN74157 (J, N)
SN54L157 (J) SN74L157 (J, N)
SN54LS157 (J, W) SN74LS157 (J, N)
SN54S157 (J, W) SN54S157 (J, N)
SN54LS158 (J, W) SN74LS158 (J, N)
SN54S158 (J, W) SN74S158 (J, N)

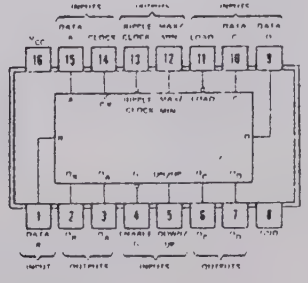
SYNCHRONOUS UP/DOWN COUNTERS

SN74LS191 S-D P/N 103982

SYNCHRONOUS UP/DOWN COUNTERS

190 BCD

191 BINARY



SN54190 (J, W) SN74190 (J, N)
SN54LS190 (J, W) SN74LS190 (J, N)
SN54191 (J, W) SN74191 (J, N)
SN54LS191 (J, W) SN74LS191 (J, N)

SN74LS196N S-D P/N 103164

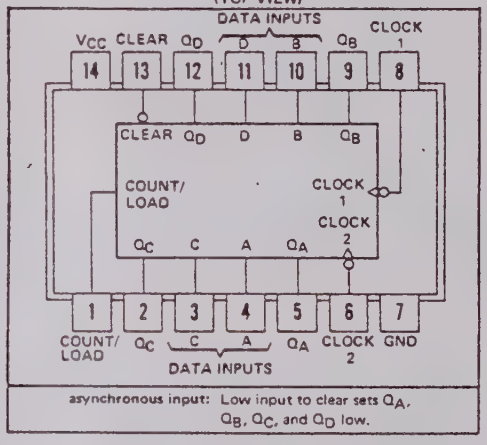
TYPES SN54196, SN54197, SN54LS196, SN54LS197, SN54S196, SN54S197, SN74196, SN74197, SN74LS196, SN74LS197, SN74S196, SN74S197
50/30/100-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

BULLETIN NO. DL-S 7711806, OCTOBER 1976—REVISED AUGUST 1977

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Input Clamping Diodes Simplify System Design
- Output Q_A Maintains Full Fan-out Capability In Addition to Driving Clock-2 Input

TYPES	GUARANTEED COUNT FREQUENCY CLOCK 1	GUARANTEED COUNT FREQUENCY CLOCK 2	TYPICAL POWER DISSIPATION
'196, '197	0-50 MHz	0-25 MHz	240 mW
'LS196, 'LS197	0-30 MHz	0-15 MHz	80 mW
'S196, 'S197	0-100 MHz	0-50 MHz	375 mW

SN54', SN54LS', SN54S' . . . J OR W PACKAGE
SN74', SN74LS', SN74S' . . . J OR N PACKAGE
(TOP VIEW)


DATA INPUTS
VCC CLEAR QD D B QB CLOCK 1
14 13 12 11 10 9 8
CLEAR QD D B QB
COUNT/ LOAD
CLOCK 1
CLOCK 2
QC C A QA
1 2 3 4 5 6 7
COUNT/ LOAD QC C A QA CLOCK 2 GND
DATA INPUTS

asynchronous input: Low input to clear sets Q_A, Q_B, Q_C, and Q_D low.

description

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops, which are internally interconnected to provide either a divide-by-two and a divide-by-five counter ('196, 'LS196, 'S196) or a divide-by-two and a divide-by-eight counter ('197, 'LS197, 'S197). These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL and DTL logic families. Series 54, 54LS, and 54S circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74, 74LS, and 74S circuits are characterized for operation from 0°C to 70°C.

typical count configurations

'196, 'LS196, and 'S196 typical count configurations and function tables are the same as those for '176. See page 7-260.
'197, 'LS197, and 'S197 typical count configurations and function tables are the same as those for '177. See page 7-260.

functional block diagrams

'196, 'LS196, and 'S196 functional block diagram is the same as that for '176. See page 7-261.
'197, 'LS197, and 'S197 functional block diagram is the same as that for '177. See page 7-261.

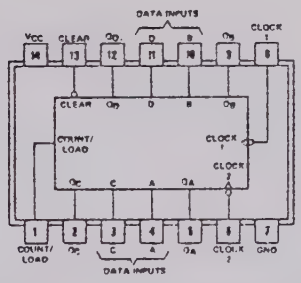
PRESETABLE COUNTERS/LATCHES

SN74LS197N S-D P/N 103165

PRESETABLE COUNTERS/LATCHES

196 DECADE/BI-QUINARY

197 BINARY



SN54196 (J, W) SN74196 (J, N)
SN54LS196 (J, W) SN74LS196 (J, N)
SN54S196 (J, W) SN74S196 (J, N)
SN54197 (J, W) SN74197 (J, N)
SN54LS197 (J, W) SN74LS197 (J, N)
SN54S197 (J, W) SN74S197 (J, N)

PROGRAMMABLE READ-ONLY MEMORIES

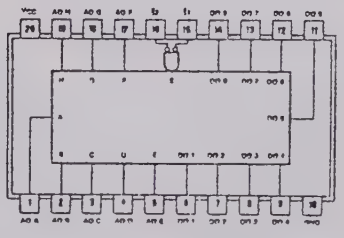
SN74S470N S-D P/N 075026

PROGRAMMABLE READ-ONLY MEMORIES

256 8-BIT WORDS

470 OPEN-COLLECTOR OUTPUTS

471 3-STATE OUTPUTS

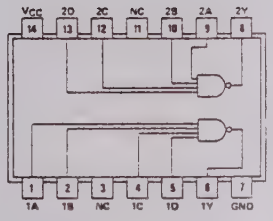


SN54S470 (J) SN74S470 (J, N)
SN54S471 (J) SN74S471 (J, N)

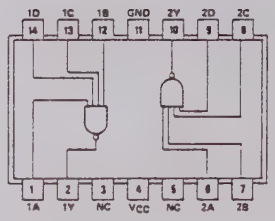
DUAL 4-INPUT POSITIVE-NAND GATES

SN7420N — S-D P/N 025713
SN74H20N — S-D P/N 045234
SN74L20N — S-D P/N 025798
SN74LS20N — S-D P/N 103969
SN74S20N — S-D P/N 106638

positive logic:
$Y = \overline{ABCD}$



SN5420/SN7420(J, N)
SN54H20/SN74H20(J, N)
SN54L20/SN74L20(J, N)
SN54LS20/SN74LS20(J, N, W)
SN54S20/SN74S20(J, N, W)



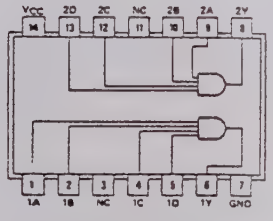
SN5420/SN7420(W)
SN54H20/SN74H20(W)
SN54L20/SN74L20(T)

NC—No internal connection

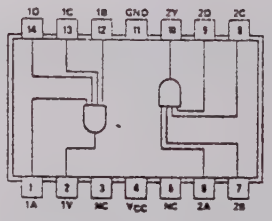
DUAL 4-INPUT POSITIVE-AND GATES

SN74LS21N — S-D P/N 103970

positive logic:
$Y = ABCD$



SN54H21/SN74H21(J, N)
SN54LS21/SN74LS21(J, N, W)



SN54H21/SN74H21 (W)

NC—No internal connection

QUAD 2-INPUT NAND
8-INPUT NAND

SN7426N
SN74LS30N

S-D P/N 045252
S-D P/N 103971

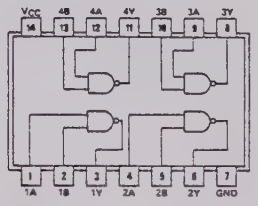
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE
POSITIVE-NAND GATES

26

positive logic:
$Y = \overline{AB}$

See pages 6-24 and 6-26



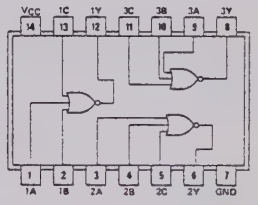
SN5426 (J)
SN54LS26 (J, W)
SN7426 (J, N)
SN74LS26 (J, N)

TRIPLE 3-INPUT
POSITIVE-NOR GATES

27

positive logic:
$Y = \overline{A+B+C}$

See page 6-3



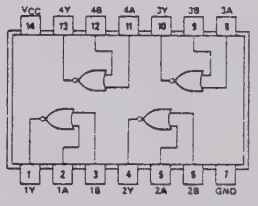
SN5427 (J, W)
SN54LS27 (J, W)
SN7427 (J, N)
SN74LS27 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-NOR BUFFERS

28

positive logic:
$Y = \overline{A+B}$

See page 6-20



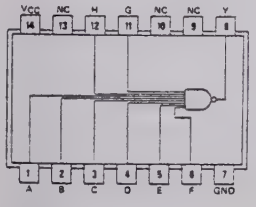
SN5428 (J, W)
SN54LS28 (J, W)
SN7428 (J, N)
SN74LS28 (J, N)

8-INPUT
POSITIVE-NAND GATES

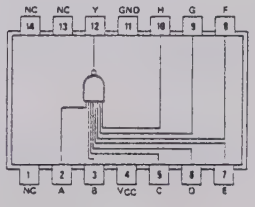
30

positive logic:
$Y = \overline{ABCDEFGH}$

See page 6-2



SN5430 (J)
SN54H30 (J)
SN54L30 (J)
SN54LS30 (J, W)
SN54S30 (J, W)
SN7430 (J, N)
SN74H30 (J, N)
SN74L30 (J, N)
SN74LS30 (J, N)
SN74S30 (J, N)



SN5430 (W)
SN54H30 (W)
SN54L30 (T)

NC—No internal connection

SN7416N

S-D P/N 045230

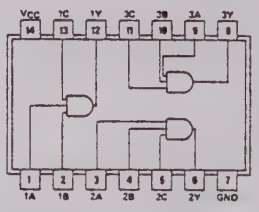
PIN ASSIGNMENTS (TOP VIEWS)

TRIPLE 3-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

15

positive logic:
Y = ABC

See page 6-12



SN54H15 (J, W)
SN54LS15 (J, W)
SN54S15 (J, W)

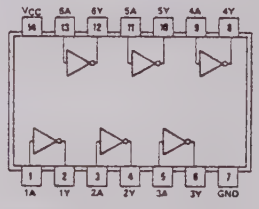
SN74H15 (J, N)
SN74LS15 (J, N)
SN74S15 (J, N)

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

16

positive logic:
Y = $\overline{A}$

See page 6-24



SN5416 (J, W)

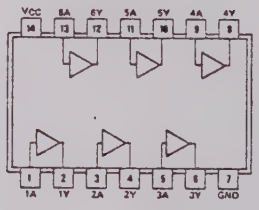
SN7416 (J, N)

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

17

positive logic:
Y = A

See page 6-24



SN5417 (J, W)

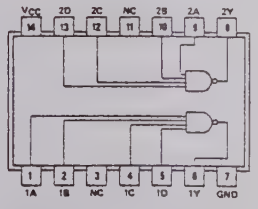
SN7417 (J, N)

DUAL 4-INPUT
POSITIVE-NAND GATES

20

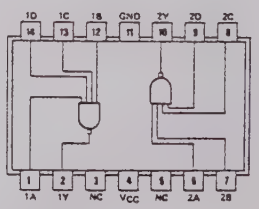
positive logic:
Y = $\overline{ABCD}$

See page 6-2



SN5420 (J)
SN54H20 (J)
SN54L20 (J)
SN54LS20 (J, W)
SN54S20 (J, W)

SN7420 (J, N)
SN74H20 (J, N)
SN74L20 (J, N)
SN74LS20 (J, N)
SN74S20 (J, N)



SN5420 (W)
SN54H20 (W)
SN54L20 (T)

NC—No internal connection

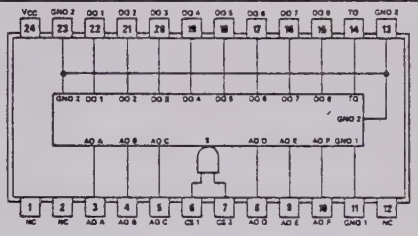
SN74188N

S-D P/N 055998

PIN ASSIGNMENTS (TOP VIEWS)

512-BIT PROGRAMMABLE READ-ONLY MEMORIES

186 64 8-BIT WORDS
OPEN-COLLECTOR OUTPUTS



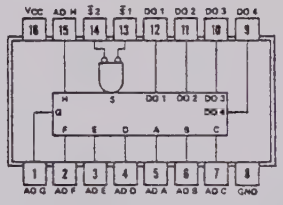
See Bipolar Microcomputer Components Data Book, LCC4270

SN54186 (J, W) SN74186 (J, N)

NC — No internal connection

1024-BIT READ-ONLY MEMORIES

187 256 4-BIT WORDS
OPEN-COLLECTOR OUTPUTS

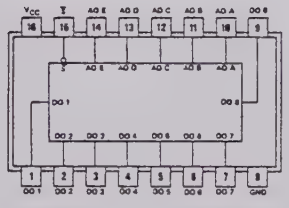


See Bipolar Microcomputer Components Data Book, LCC4270

SN54187 (J, W) SN74187 (J, N)

256-BIT PROGRAMMABLE READ-ONLY MEMORIES

188 32 8-BIT WORDS
OPEN-COLLECTOR OUTPUTS

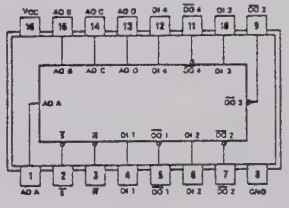


See Bipolar Microcomputer Components Data Book, LCC4270

SN54188A (J, W) SN74188A (J, N)
SN54S188 (J, W) SN74S188 (J, N)

64-BIT RANDOM-ACCESS MEMORIES

189 16 4-BIT WORDS
THREE-STATE OUTPUTS



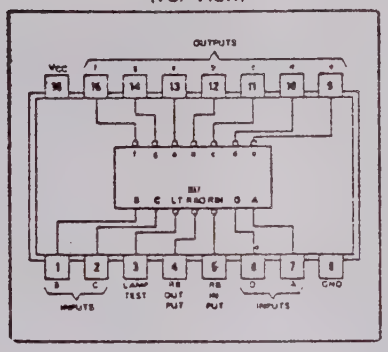
See Bipolar Microcomputer Components Data Book, LCC4270

SN54S189 (J, W) SN74S189 (J, N)

SN74247N
SN74LS247

S-D P/N 103314
S-D P/N 103166

'246, '247, 'LS247
(TOP VIEW)

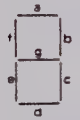


description

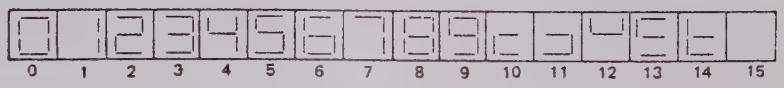
The '246 through '248 are electrically and functionally identical to the SN5446A/SN7446A, SN5447A/SN7447A, and SN5448/SN7448, respectively, and have the same pin assignments as their equivalents. Also the 'LS247 and 'LS248 are electrically and functionally identical to the SN54LS47/SN74LS47 and SN54LS48/SN74LS48, respectively, and have the same pin assignments as their equivalents. They can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The '249 and 'LS249 are 16-pin versions of the 14-pin SN5449 and SN54LS49/SN74LS49, respectively. Included in the '249 and 'LS249 circuits is the full functional capability for lamp test and ripple blanking, which is not available in the '49 and 'LS49 circuits. The '46A, '47A, '48, '49, 'LS47, 'LS48, and 'LS49 compose the 6 and the 9 without tails and the '246 through '249 and 'LS247, 'LS248, and 'LS249 compose the 6 and the 9 with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The '246, '247, and 'LS247 feature active-low outputs designed for driving indicators directly, and the '248, '249, 'LS248, and 'LS249 feature active-high outputs for driving lamp buffers. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

All of these circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

Series 54 and Series 54LS devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and Series 74LS devices are characterized for operation from 0°C to 70°C.



SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

SN74247N
SN74LS247

S-D P/N 103314
S-D P/N 103166

'246, '247, 'LS247
FUNCTION TABLE

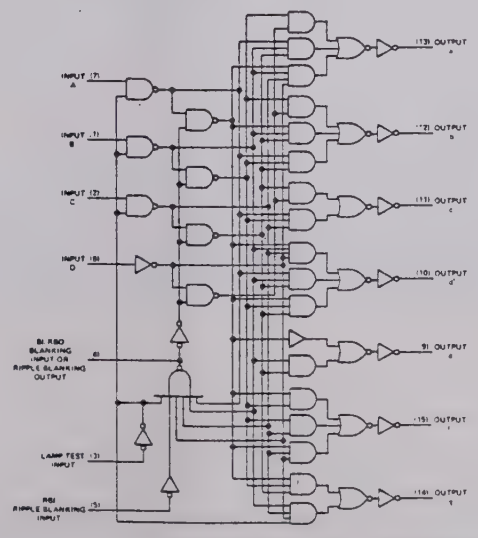
DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES:
1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

'246, '247, 'LS247



SN75451AP S-D P/N 045290

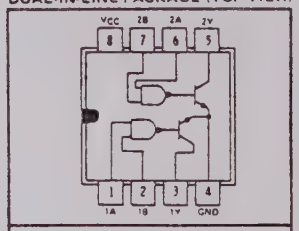
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

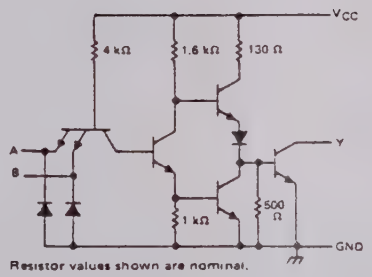
H = high level, L = low level

SN55451B . . . JG
SN75451B . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = AB

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN55451B			SN75451B			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 30 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		7	11		7	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		52	65		52	65	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		18	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			18	25	ns
t_{TLH}	Transition time, low-to-high-level output			5	8	ns
t_{THL}	Transition time, high-to-low-level output			7	12	ns
V_{OH}	High-level output voltage after switching	V_S = 20 V, I_O ≈ 300 mA, See Figure 4	V_S−6.5			mV

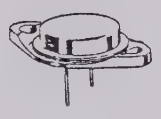
MC7805CT

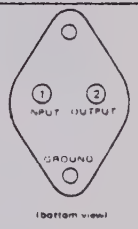
S-D P/N 045256

MC7800C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC7800C Series of three-terminal positive voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. Available in seven fixed output voltage options from 5.0-to-24 volts, these regulators employ internal current limiting, thermal shutdown, and safe area compensation — making them essentially blow-out proof. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. The last two digits of the part number indicate nominal output voltage.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 313 and Case 11 (TO-220 and Hermetic TO-3)





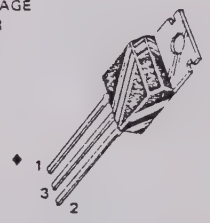
(bottom view)

K SUFFIX
METAL PACKAGE
CASE 11-01
(TO-3 TYPE)

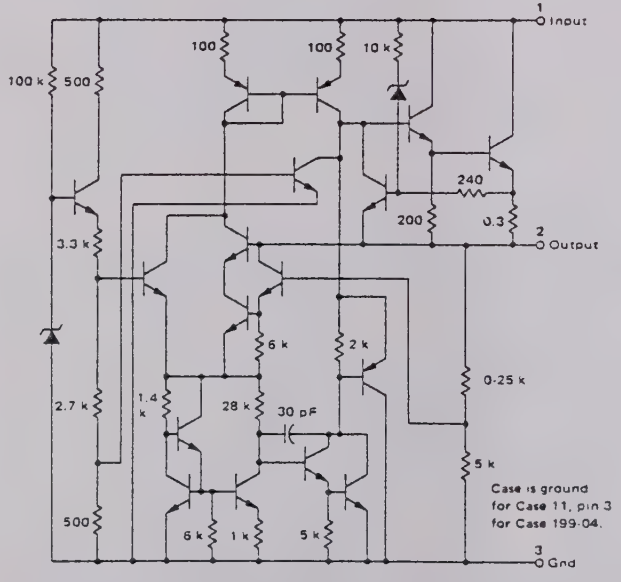
Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

T SUFFIX
PLASTIC PACKAGE
CASE 313
TO-220

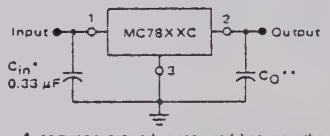
1 Input
2 Output
3 Ground



SCHEMATIC DIAGRAM



♦ STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

TYPE NO./VOLTAGE

MC7805C 5.0 Volts	MC7808C 8.0 Volts	MC7818C 18 Volts
MC7806C 6.0 Volts	MC7812C 12 Volts	MC7824C 24 Volts
	MC7815C 15 Volts	

ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC78XXCK	T_J = 0° C to +150° C	Metal Power
MC78XXCT	T_J = 0° C to +150° C	Plastic Power

MC7900C SERIES THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

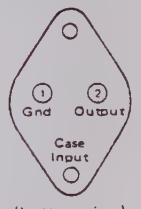
The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven-voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.

Available in fixed output voltage options from -2.0 to -24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A and Case 1 (TO-220 and Hermetic TO-3)

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

K SUFFIX
METAL PACKAGE
CASE 1
(TO-3 TYPE)



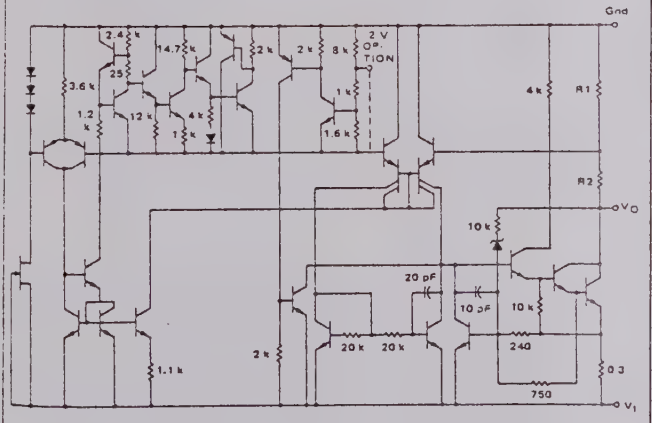
(bottom view)

T SUFFIX
PLASTIC PACKAGE
CASE 221A

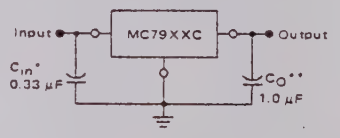
Pin 1. Ground
2. Input
3. Output

(Heatsink surface connected to Pin2)

SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7902C - 2.0 Volts	MC7906C - 6.0 Volts	MC7915C - 15 Volts
MC7905C - 5.0 Volts	MC7908C - 8.0 Volts	MC7918C - 18 Volts
MC7905.2C — 5.2 Volts	MC7912C - 12 Volts	MC7924C - 24 Volts

ORDERING INFORMATION

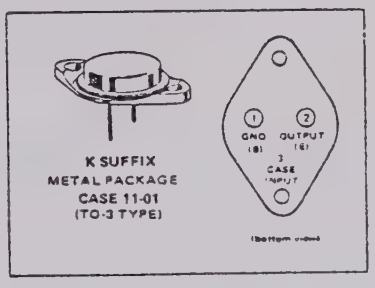
DEVICE	TEMPERATURE RANGE	PACKAGE
MC79XXCK	T_J = 0° C to +150° C	Metal Power
MC79XXCT	T_J = 0° C to +150° C	Plastic Power

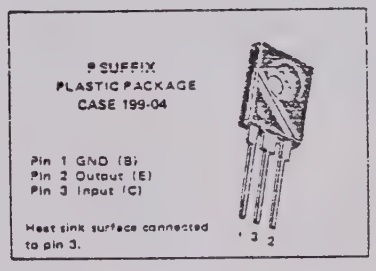
XX indicates nominal voltage

MC7900C SERIES THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

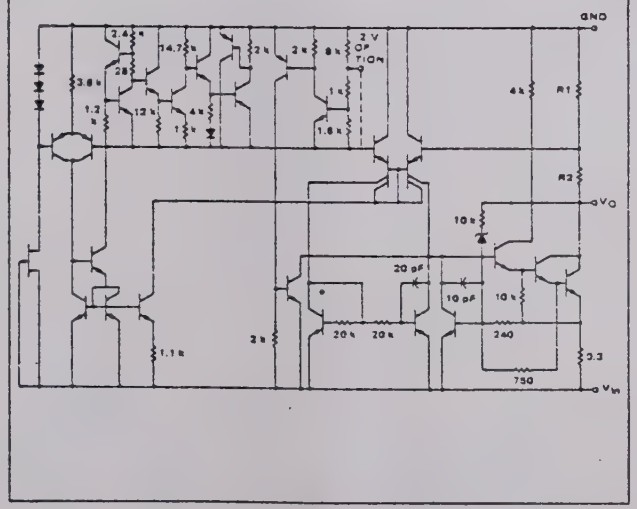
The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven-voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.

Available in fixed output voltage options from -2.0 to -24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation – making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.





SCHEMATIC DIAGRAM



DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7902C - 2.0 Volts	MC7906C - 6.0 Volts	MC7915C - 15 Volts
MC7905C - 5.0 Volts	MC7908C - 8.0 Volts	MC7918C - 18 Volts
MC7905.2C - 5.2 Volts	MC7912C - 12 Volts	MC7924C - 24 Volts

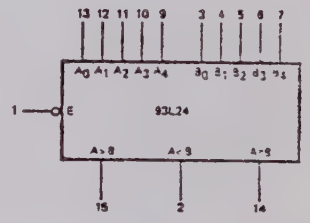
LOW POWER 5-BIT COMPARATOR

93L24PC **S-D P/N 117020**

DESCRIPTION — The LPTTL/MSI 93L24 is a Medium Speed Expandable Comparator which provides comparison between two 5-bit words and gives three outputs, "less than", "greater than", and "equal to". A HIGH level on the active LOW enable input forces all three outputs LOW.

- THREE SEPARATE OUTPUTS . . . A < B, A > B, A = B
- EASILY EXPANDABLE
- ACTIVE LOW-LEVEL ENABLE INPUT
- HIGH DRIVE OUTPUT CIRCUITRY
- TYPICAL PROPAGATION DELAY OF 55 ns (A > B)
- TYPICAL POWER DISSIPATION OF 52 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

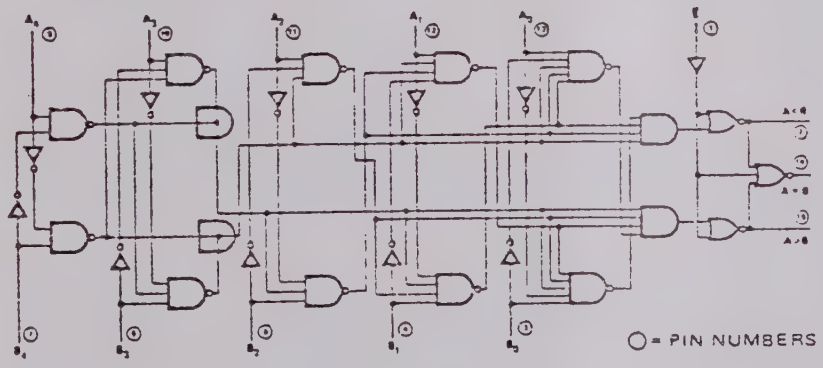
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

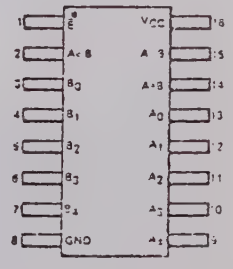
CONNECTION DIAGRAMS
DIP (TOP VIEW)

LOGIC DIAGRAM



○ = PIN NUMBERS

FLATPAK(TOP VIEW)



PIN NAMES

		LOADING HIGH	LOADING LOW
$\bar{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
A_0, A_1, A_2, A_3, A_4	Word A Parallel Inputs	1.0 U.L.	0.5 U.L.
B_0, B_1, B_2, B_3, B_4	Word B Parallel Inputs	1.0 U.L.	0.5 U.L.
A < B	A Less than B Output	9 U.L.	2.25 U.L.
A > B	A Greater than B Output	9 U.L.	2.25 U.L.
A = B	A Equal to B Output	10 U.L.	2.5 U.L.

FUNCTIONAL DESCRIPTION – The 93L24 5-bit comparator uses combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three output are activated by the active LOW enable input ($\overline{E}$).

Tying the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion as shown in Figure 1.

The A_4 and B_4 inputs are the most significant inputs and A_0, B_0 the least significant. Thus if A_4 is HIGH and B_4 is LOW, the A > B output will be HIGH regardless of all other inputs except $\overline{E}$.

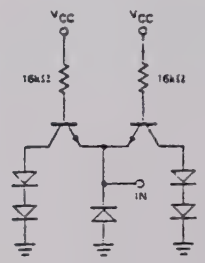
TRUTH TABLE

$\overline{E}$	A B	A < B	A > B	A = B
H	X X	L	L	L
L	Word A = Word B	L	L	H
L	Word A > Word B	L	H	L
L	Word A < Word B	H	L	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Either HIGH or LOW Voltage Level

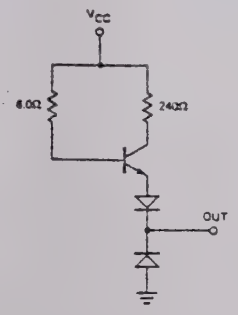
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT

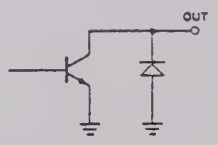


OUTPUTS EQUIVALENT CIRCUITS

OUTPUT HIGH



OUTPUT LOW



CHAPTER 6

REPLACEABLE PARTS

6.1 INTRODUCTION

This chapter contains the spare parts lists for the assemblies that comprise the 604XA Frequency Counters. Assembly drawings in Chapter 7 show the physical location of parts/components. The parts ordering information in paragraph 6.2 will expedite your order if followed. An explaination of the parts list columns is provided in paragraph 6.3.

6.2 PART ORDERING INFORMATION

To order a part from the Replacement Parts List, state the Systron-Donner part number and description, indicate the quantity required and address the order to the nearest Systron-Donner sales or service center.

To order a part not listed in the Replacement Parts List, state the instrument model number, instrument serial number, the description and function of the part and the number of parts required. Address the order to the nearest Systron-Donner sales or service center.

6.3 PARTS LIST

The replacement parts lists are placed in A numbered sequence.

Each column in the parts lists provide specific information relating to the listed parts as follows:

(1) DESIGNATOR: Circuit reference numbers are listed alpha-numerically.

(2) COMPONENT NOMENCLATURE AND DESCRIPTION: Component names and specifications are provided in this column and include value, tolerance, working voltage, wattage rating, construction, etc.

(3) MANUFACTURER'S CODE: H4-2 Federal Supply Code numbers for manufacturers are listed in this column to identify component manufacturer. Table 6-1 is provided in this chapter for number to name cross reference.

(4) MANUFACTURER'S PART NUMBER: True manufacturer part numbers are listed in this column. In those instances when more than one manufacturer's part is available, the part number is typical.

(5) SD STOCK NUMBER: The Systron-Donner part (stock) number is listed in this column.

(6) T/Q (Total Quantity): This quantity, appearing after an item entry, indicates the number of times the component is used in that assembly. The total quantity for each part is given only once - at the first appearance of the part number is the list.

TABLE 6.1 MANUFACTURER'S CODE-TO-NAME INDEX

CODE	NAME
00779	AMP Inc. P.O. Box 3608 Harrisburg, PA. 17105
01121	Allen-Bradley Company 1201 So. 2nd Street Milwaukee, WI. 53204
01295	Texas Instruments Inc. Semiconductor & Comp. Div. 13500 No. Central Expressway Dallas, TX. 75231
02660	Bunker Ramo Corporation Amphenol Connector Div. 2801 So. 25th Avenue Broadview, IL. 60153
02735	RCA Corporation Solid State Division Route 202 Somerville, NJ. 08876
02763	Grippe Machining & Mfg. Co. 15642 Common Road Roseville, MI. 48066
03508	General Electric Company Semiconductor Prod. Dept. Electronics Park Syracuse, NY. 13201
04713	Motorola Semiconductor Prod.Inc. 5005 E. McDowell Road Phoenix, AZ. 85008
06383	Panduit Corporation 17301 Ridgeland Tinley Park, IL. 60477
06540	Amatom Electronic Hardware Division of Mite Corp. 81 Rockdale Avenue, New Rochelle, NY. 10806
07263	Fairchild Camera & Instr. Corp. Semiconductor Division 313 Frontage Road Mountain View, CA. 94040
08289	Blinn Delbert Co. Inc, The P.O. Box 2007 1678 Mission Blvd., Pomona, CA. 91766
15818	Teledyne Semiconductor 1300 Terra Bella Avenue Mountain View, CA. 94040
16733	Phelps Dodge Communication Co. Div. of Phelps Dodge Copper Prod. Corp. North Haven, CT. 06473
18324	Signetics Corporation 811 E. Arques Sunnyvale, CA. 94086
21847	Aertech 825 Stewart Drive Sunnyvale, CA. 94086
26654	Varadyne Inc. Capacitor Division 2110 Broadway Santa Monica, CA. 90404
27018	Optimum Designs Inc. 152 W. 42nd Street New York, NY. 10017
27264	Molex Products Company 5224 Katrine Avenue Downers Grove, IL. 60515
27556	IMB Electronic Prod. Inc. 15401-E Carmenita Road Santa Fe Springs, CA. 90670
28480	Hewlett-Packard Company 1501 Page Mill Road Palo Alto, CA. 94304
30146	A P Inc. 72 Corwin Drive Painesville, OH. 44077
31918	International Electro Exch. Inc. 8081 Wallace Road Eden Prairie, NM. 55343
32159	West-Cap Arizona 2201 E. Elvira Road Tucson, AZ. 85706
34420	Verdyne Corporation 330 No. Victory Blvd., Burbank, CA. 91502

TABLE 6.1 MANUFACTURER'S CODE-TO-NAME INDEX

CODE	NAME
50522	Monsanto Company Electronic Special Products 10131 Bubb Road Cupertino, CA. 95014
52542	Systron-Donner Corporation Instrument Division 10 Systron Drive Concord, CA. 94518
52648	Plessey Semiconductor 1674 McGaw Avenue Santa Ana, CA. 92705
56289	Sprague Electronic Company North Adams, MA. 01247
71279	Cambridge Thermonic Corporation 445 Concord Avenue Cambridge, MA 01238
71590	Globe-Union Inc. Centralab Electronics Div. 5757 No. Green Bay Avenue Milwaukee, WI. 53201
72136	Electro Motive Mfg. Co. Inc. South Park & John Sts., Willimantic, CO. 06226
72259	Nytronics Inc. 10 Pelham Parkway Pelham Mannor, NY. 10803
72982	Erie Technological Prod. Inc. 644 W. 12th Street Erie, PA. 16512
73138	Beckman Instruments Inc. Helipot Div. 2500 Harbor Blvd., Fullerton, CA. 92634
73734	Federal Screw Prod. Inc. 3917 N. Kenzie Ave., Chicago, IL. 60618
73803	Texas Instruments Inc. Metallurigical Materials Div. Attleboro, MA. 02703
75915	Littlefuse Inc. 800 E. Northwest Highway Des Plaines, IL. 60016
78189	Illinois Tool Works Inc. Shakeproof Division St. Charles Road Elgin, IL. 60120
78553	Tinnerman Products Inc. 8700 Brookpark Road Cleveland, OH. 44129
79963	Zierick Mfg. Company Radio Circle Mt. Kisco, NY. 10549
80294	Bourns Inc. Instrument Div. 6135 Magnolia Avenue Riverside, CA. 92506
81073	Grayhill Inc. 561 Hillgrove Avenue La Grange, IL. 60525
81349	MID STD
81483	International Rectifier Corp. 9220 Sunset Blvd., Los Angeles, CA. 90069
82389	Switchcraft Inc. 5555 N. Elston Avenue Chicago, IL. 60630
83330	Smith, Herman H. Inc. 812 Snediker Avenue Brooklyn, NY. 11207
86928	Seastrom Mfg. Co. Inc. 701 Sonora Avenue Glendale, CA. 91201
88245	Litton Systems Inc. USECO Division 13536 Saticoy Street Van Nuys, CA. 91409
91418	Radio Materials Company 4242 W. Bryn Mawr Chicago, IL. 60646

TABLE 6.1 MANUFACTURER'S CODE-TO-NAME INDEX

CODE	NAME
95987	Weckesser Co. Inc. 4444 W. Irving Park Road Chicago, IL. 60641
96906	MIL STD
98291	Sealectro Corporation 225 Hoyt Mamaroneck, NY. 10544
98921	O and M Mfg. Company 8203 Market Street Road Houston, TX. 77029
98978	Int'l Electronic Research Corp 135 W. Magnolia Avenue Burbank, CA. 91502
99392	S T M Corporation 2904 Champman Street Oakland, CA. 94601
99515	ITT Jennings Monrovia Plant Div. of ITT Jennings 1960 Walker Avenue Monrovia, CA. 91016

REPLACEABLE PARTS LIST

TITLE 604XA SHIPPING ASSEMBLY REV A

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
		ASSEMBLY, Shipping 6041A	52542	067669	067669	1
		ASSEMBLY, Shipping 6042A	52542	067670	067670	1
		ASSEMBLY, Shipping 6043A	52542	067671	067671	1
		ASSEMBLY, Test 6041A	52542	067668	067668	1
		ASSEMBLY, Test 6042A	52542	067287	067287	1
		ASSEMBLY, Test 6043A	52542	067288	067288	1
		PANEL, Decorative 6041A	52542	067567	067567	1
		PANEL, Decorative 6042A	52542	067286	067286	1
		PANEL, Decorative 6043A	52542	067207	067207	1
		WINDOW	52542	067231	067231	1
		TRIM, Top & Bottom	52542	057700	057700	2
		COVER, Top & Bottom	52542	067388	067388	2
		RACK, Ear Mtg.	52542	057979	057979	2
		CORD, Line	70903	BR-1736	102407	1

REPLACEABLE PARTS LIST

TITLE 604XA TEST ASSEMBLY REV A

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
		ASSEMBLY, Test 6041A	52542	067668	067668	Ref
		ASSEMBLY, Test 6042A	52542	067287	067287	Ref
		ASSEMBLY, Test 6043A	52542	067288	067288	Ref
1		ASSEMBLY, Universal Chassis	52542	067486	067486	1
2	A1	ASSEMBLY, 512 MHz Prescaler PC 6042A only	52542	06729901	06729901	1
2	A1	ASSEMBLY, 1.25 GHz Prescaler PC 6043A only	52542	06725001	06725001	1
3		BRACKET, Front	52542	057951	057951	1
5		BRACKET, Prescaler Mtg 6042A & 6043A	52542	067260	067260	1
6	J1	BNC,Fused 6042A & 6043A	16733	CD701938-002	117080	1
7		SCREW, 8-32 x ½ FHMS	96906	MS24693-C50	10074308	1
8		SCREW, 6-32 x 5/16 PHMS 6042A & 6043A	96906	MS51957-27	10063205	4
10		SCREW, 4-40 x 3/8 FHMS 6041A only	96906	MS24693-C4	10072006	2
10		SCREW, 4-40 x 7/16 FHMS 6042A & 6043A	96906	MS24693-C5	10072007	2
11		WASHER, #6 Flat 6042A & 6043A	86928	5710-23-10	100662	4
12		WASHER, #6 Split 6042A & 6043A	96906	MS35338-136	100712	4
13		WASHER, #8 Split 6042A & 6043A	96906	MS35338-137	100713	1
14		NUT, Kep 8-32 6041A	78189	511-041800-00	100940	1
14		NUT, 8-32 Small Pattern 6042A & 6043A	73734	70208	100659	1

REPLACEABLE PARTS LIST

TITLE	604XA UNIVERSAL CHASSIS ASSEMBLY 067486 REV B (Fig 7-1)					
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
1	A2	ASSEMBLY, Logic PC	52542	06725201	06725201	1
2	A3	ASSEMBLY, IEEE 488 PC	52542	06720301	06720301	1
3		ASSEMBLY, Oscillator PC	52542	05746802	05746802	1
5	A4	ASSEMBLY, Readout PC	52542	06722901	06722901	1
6	A5	ASSEMBLY, IEEE Output PC	52542	06722601	06722601	1
7		ASSEMBLY, Rear Panel	52542	067395	067395	1
8	T1	TRANSFORMER	52542	067137	067137	1
9		PANEL, Right Side	52542	055747	055747	1
10		PANEL, Left Side	52542	057978	057978	1
11		BRACKET, Center	52542	067006	067006	1
12		BRACKET, Side	52542	057952	057952	1
13		BRACKET, Front	52542	057951	057951	1
15		Sub-Panel	52542	067208	067208	1
16		Pushbotton, Gray	31918	FSC GRAY	117291	10
17		Pushbutton, Red	31918	FG RED	117256	1
19	J2	CONNECTOR, BNC	81349	UG1094/U	101155	1
20		LUG, 3/8 ID, ½ OD x 2L	79963	334-375	112551	1
22		STUD, Connector Mtg	52542	057361	057361	2
23	P1,2,4	CABLE, Ribbon 8"	30146	922521-20-02-8	117210	3
24	P3	CABLE, Ribbon 14"	30146	922521-20-02-14	117401	1
25	S1	SWITCH, 13 Pos. pushbutton	52542	067284	067284	1
31		SCREW, 8-32 x ½ FHMS	96906	MS24693-C50	10074308	1
32		SCREW, 8-32 x 7/8 PHMS	96906	MS51957-48	10064214	4
34		SCREW, 6-32 x 5/16 PHMS	96906	MS51957-27	10063205	4
35		SCREW, 6-32 x 3/8 PHMS	96906	MS51957-28	10063206	4
36		SCREW, 6-32 x 7/16 FHMS	96906	MS24693-C27	10073107	11
38		SCREW, 4-40 x 3/8 FHMS	96906	MS24693-C4	10072006	2
39		SCREW, 4-40 x 5/16 PHMS	96906	MS51957-14	10062605	8
42		SCREW, 2-56 x ¼ PHMS	96906	MS51957-3	10062504	4
43		CABLE, Tie	06383	SSTIM	100753	A/R
44		WASHER, #2 Flat	96906	MS15795-802	100614	2
45		WASHER, #2 Split	96906	MS35337-77	100661	4

REPLACEABLE PARTS LIST

TITLE 604XA UNIVERSAL CHASSIS ASSEMBLY 067486 (Cont'd)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
46		WASHER, #4 Flat	96906	NAS620-42	100683	8
47		WASHER, #4 Split	96906	MS35338-135	100711	8
48		WASHER, #6 Flat	86928	5710-23-10	100662	8
49		WASHER, #6 Split	96906	MS35338-136	100712	8
50		WASHER, #8 Flat	86928	5702-225-30-C1	103014	4
51		WASHER, #8 Split	96906	MS35338-137	100713	2
52		NUT, Kep 8-32	78189	511-081800-00	100940	5
53		NUT, Hex 6-32 Small Pattern	96906	NAS671C6	100638	1
54		NUT, Speed 6-32	78553	C10293SS-632-24	101123	4
55		TIE, Anchor	06383	TMIS 6	102748	2
56		CABLE, Clamp 3/16	95987	3/16	102931	1
57		CLIP, Heatsink P/O 117254	98978	PVC-1B	117255	1
58		HEATSINK	98978	PA1-7CB	117254	1

REPLACEABLE PARTS LIST

TITLE 604XA REAR PANEL ASSEMBLY 067395 REV A (Fig 7-2)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
1		PANEL, Rear	52542	067209	067209	1
2		HEATSINK, Regulator	52542	067321	067321	1
3	T2	TRANSFORMER	52542	057961	057961	1
4	J3, 4	CONNECTOR, BNC	81349	UG-1094/U	101155	2
5	U34, 56	INTEGRATED CIRCUIT 5V Voltage Regulator	04713	MC7805CP	045256	2
6	U35	INTEGRATED CIRCUIT 5.2V Voltage Regulator	04713	MC7905.2CP	103033	1
7	J5	CONNECTOR	82389	EAC-301	101288	1
8	XF1	FUSE, Post	75915	345001	117377	1
9	F1	FUSE, .375A	75915	323.375	100604	1
10	S2	SWITCH, Pushbutton	81073	30-1	102313	1
11		PLUG, Button 3/8	83330	652	100840	1
12		PLUG, Button 1/2	83330	653	100904	1
13		LUG, BNC	79963	814	107077	1
14		LUG, #4	83330	1416-4	100509	1
15		SCREW, 8-32 x 5/16 PHMS	96906	MS51957-42	10064205	2
16		SCREW, 6-32 x 3/8 FHMS	96906	MS24693-C26	10073106	2
17		SCREW, 4-40 x 3/8 PHMS	96906	MS51957-15	10062606	2
18		SCREW, 4-40 x 5/16 PHMS	96906	MS51957-14	10062605	3
19		WASHER, #4 Flat	96906	MS15795-803	100703	3
20		WASHER, #4 Split	96906	MS35338-135	100711	4
21		WASHER, #6 Split	96906	MS35338-136	100712	2
22		WASHER, Shoulder	02735	DF137A	103397	1
23		INSULATOR	08289	SK-73-48-13	103352	1
24		NUT, Kep 8-32	78189	511-081800-00	100940	2
25		NUT, Cap 6-32	73734	8061-NP	103059	2
26		NUT, Hex 4-40	96906	NAS671C4	100622	5
27		NUT, Speed 6-32	78553	C10293SS-632-24	101123	6

REPLACEABLE PARTS LIST

TITLE 6042A 512 MHz PRESCALER (A1) ASSEMBLY 0672990l REV B (Fig 7-7,7-8)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	C1 thru C11	CAPACITOR, Ceramic Chip .056 µF 20%, 100V	32159	SC31BX563M	100257	18
	C12 thru C15	CAPACITOR, Ceramic Chip 15 pF 5%	32159	SC23BY150JP	100256	5
	C16	CAPACITOR, Ceramic Chip 5.1 pF 100V	32159	SC25BY5R1D	100270	1
	C17 thru C20	Same as C1				
	C21	Same as C12				
	C22 thru C24	Same as C1				
	C25	CAPACITOR, Ceramic Disc 1 µF 20%, 50V	56289	5CZ5U105X0050C5	100176	1
	C26	CAPACITOR, Tant 10 µF 10%, 20V	56289	150D106X9020B2	100063	2
	C27	CAPACITOR, Ceramic Disc .05 µF +80-20%, 10V	71590	UK10-503	100122	2
	C28	Same as C26				
	C29	Same as C27				
	CR1	DIODE, Mixer Det	28480	A2X1619	100437	2
	CR2	DIODE, Pin	21847	A5S138	103197	1
	CR3	DIODE, Utra Fast Switch	28480	5082-2800	100442	2
	CR4	Same as CR3				
	CR5	Same as CR1				
	CR6	DIODE	28480	5082-2810	103346	2
	CR7	Same as CR6				
	L1 thru L4	INDUCTOR 10 µH 10%	72259	WEE-WEE-10	101317	4
	P1	ASSEMBLY, Input Cable	52542	067290	067290	1
	P2	ASSEMBLY, Output Cable	52542	067347	067347	1
	Q1 thru Q4	TRANSISTOR, SINPN	04713	2N6304	103171	4

REPLACEABLE PARTS LIST

TITLE 6042A 512 MHz PRESCALER (A1) ASSEMBLY 0672990l (Cont'd)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	Q5	TRANSISTOR, SIPNP	04713	2N3906	101378	1
	R1	RESISTOR, CC 68 Ω 5%, 1/4W	01121	CB6805	101690	1
	R2 thru R5	RESISTOR, CC 68 Ω 5%, 1/8W	01121	BB6805	101700	4
	R6 thru R9	RESISTOR, CC 22 Ω 5%, 1/4W	01121	BB2205	101696	4
	R10	RESISTOR, CC 56 Ω 5%, 1/8W	01121	BB5605	101816	1
	R11	RESISTOR, CC 330 Ω 5%, 1/8W	01121	BB3315	101704	1
	R12	RESISTOR, CC 470 Ω 5%, 1/4W	01121	CB4715	101625	1
	R13	RESISTOR, CC 100 k 5%, 1/4W	01121	CB1045	101558	1
	R14	RESISTOR, CC 10 k 5%, 1/4W	01121	CB1035	101570	2
	R15	Same as R14				
	R16	RESISTOR, CC 1 k 5%, 1/4W	01121	CB1025	101569	2
	R17	RESISTOR, CC 560 Ω 5%, 1/4W	01121	CB5615	101583	1
	R18	RESISTOR, CC 4.7 k 5%, 1/4W	01121	CB4725	101598	1
	R19	RESISTOR, Variable 1 k 20%, 1/2W	80294	3329H-1-102	101919	1
	R20	RESISTOR, CC 5.1 k 5%, 1/4W	01121	CB5125	101541	1
	R21	Same as R16				
	R22	RESISTOR, CC 1.5 M 5%, 1/4W	01121	CB1555	101659	1
	TP1	FEED THRU, Teflon	98921	001-1007	100575	1
	U1	INTEGRATED CIRCUIT 700 MHz counter	52648	SP8613B	117475	1

REPLACEABLE PARTS LIST

TITLE	6042A 512 MHz PRESCALER (A1) ASSEMBLY 06729901 (Cont'd)				
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	U2	INTEGRATED CIRCUIT, LIN Diff. Voltage Component	01295	SN72311P	103943	1
		WASHER, Mylar	86928	5622-9-7	100921	4
		PC BOARD	52542	067299	067299	

REPLACEABLE PARTS LIST

TITLE 6043A 1.25 GHz PRESCALER (A1) ASSEMBLY 06725001 REV C (Fig 7-9,7-10)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	C1 thru C4	CAPACITOR, Ceramic Chip .01 µF 20%, 50V	26654	2BX050S103MD	106509	23
	C5	CAPACITOR, Variable 1-5 pF 100V	72982	513-002A1-5pF	103935	2
	C6 thru C10	Same as C1				
	C11	CAPACITOR, Ceramic Chip 5.1 pF 100V	32159	SC25BY5R10	100270	5
	C12 thru C15	Same as C1				
	C16	Same as C5				
	C17	Same as C11				
	C18	Same as C11				
	C19	Same as C5				
	C20	Same as C11				
	C21	Same as C11				
	C22 thru C30	Same as C1				
	C31	CAPACITOR, Tant 10 µF 10%, 20V	56289	150D106X9020B2	100063	2
	C32	Same as C31				
	C33	CAPACITOR, Ceramic Disc 1 µF 20%, 50V	56289	5CZ5U105X0050C5	100176	1
	C34	CAPACITOR, Ceramic Disc .05 µF 10V +80-20%	71590	UK10-503	100122	2
	C35	Same as C34				
	CR1	DIODE, Mixer Det	28480	A2X1619	100437	2
	CR2	DIODE, Pin	21847	A5S138	103197	1
	CR3	DIODE, Ultra Fast Switch	28480	5082-2800	100442	2
	CR4	Same as CR3				

REPLACEABLE PARTS LIST

TITLE 6043A 1.25 GHz PRESCALER (A1) ASSEMBLY 06725001 (Cont'd)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	P1	ASSEMBLY, Input Cable	52542	067290	067290	1
	P2	ASSEMBLY, Output Cable	52542	067347	067347	1
	Q1 thru Q4	TRANSISTOR, SINPN	04713	BFR90	103948	4
	Q5	TRANSISTOR, SIPNP	04713	2N3906	101378	1
	R1	RESISTOR, CC 68 Ω 5%, 1/4W	01121	CB6805	101690	2
	R2	RESISTOR, CC 56 Ω 5%, 1/4W	01121	CB5605	101735	3
	R3	RESISTOR, Chip 22 Ω 5%	34420	1C220J	103998	5
	R4	Same as R2				
	R5	Same as R3				
	R6	Same as R2				
	R7	Same as R3				
	R8	Same as R1				
	R9	Same as R3				
	R10	RESISTOR, CC 330 Ω 5%, 1/4W	01121	CB3315	101704	1
	R11	RESISTOR, CC 470 Ω5%, 1/4W	01121	CB4715	101625	1
	R12	RESISTOR, CC 100 k 5%, 1/4W	01121	CB1045	101558	1
	R13	Same as R3				
	R14	RESISTOR, Chip 50 Ω 1%	34420	2C500F	101991	1
	R15	RESISTOR, Variable 50 Ω 20%, 1/2W	73138	62PR50	101906	1
	R16	RESISTOR, CC 560 Ω 5%, 1/4W	01121	CB5615	101583	2
	R17	Same as R16				
	R18	RESISTOR, CC 10 k 5%, 1/4W	01121	CB1035	101570	2

REPLACEABLE PARTS LIST

TITLE 6043A 1.25 GHz PRESCALER (A1) ASSEMBLY 06725001 (Cont'd)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	R19	Same as R18				
	R20	RESISTOR, CC 1 k 5%, 1/4W	01121	CB1025	101569	2
	R21	RESISTOR, CC 4.7 k 5%, 1/4W	01121	CB4725	101598	1
	R22	RESISTOR, Variable 1 k 20%, 1/2W	80294	3329H-1-102	101919	1
	R23	RESISTOR, CC 1.5 M 5%, 1/4W	01121	CB1555	101659	1
	R24	RESISTOR, CC 5. 1 k 5%, 1/4W	01121	CB5125	101541	1
	R25	Same as R20				
	R26	RESISTOR, CC 120 Ω 5%, 1/8W	01121	BB1215	101970	1
	TP	FEED THRU, Teflon	98921	001-1007	100575	1
	U1	INTEGRATED CIRCUIT, ECL 1.3 GHz Divider	52648	SP8617B	117476	2
	U2	Same as U1				
	U3	INTEGRATED CIRCUIT, LIN Diff. Voltage Component	01295	SN72311P	103943	1
		PC BOARD	52542	067250	067250	1

REPLACEABLE PARTS LIST

TITLE 604XA LOGIC (A2) ASSEMBLY 06725201 REV D (Fig 7-11,7-12)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	C1	CAPACITOR, Met Mylar .1 µF 10%, 600V	27556	ZR2G104K	117506	1
	C2	CAPACITOR, Dip Mica 10 pF 5%, 500V	72136	DM10CD100JO	100272	3
	C3	Same as C2				
	C4	CAPACITOR, Dip Mica 100 pF 5%, 500V	72136	DM10FD101JO	100252	1
	C5	CAPACITOR, Dip Mica 1000 pF 5%, 100V	72136	DM15FA102JO1CRT	100370	1
	C6	CAPACITOR, Tant 100 µF 10%, 10V	56289	196D107X9010PA1	103714	2
	C7	CAPACITOR, Tant 1 µF 10%, 35V	56289	196D105X9035HA1	103716	6
	C8	CAPACITOR, Ceramic Mold .001 µF 20%, 50V	71590	CW15C102M	100251	2
	C9	Same as C6				
	C10	CAPACITOR, Ceramic Disc 2 pF 10%, 500V	91418	Type C	100053	1
	C11	CAPACITOR, Dip Mica 56 pF 5%, 500V	72136	DM15ED560JO	100179	1
	C12	CAPACITOR, Tant 10 µF 10%, 10V	56289	196D106X9020JA1	103715	1
	C13	CAPACITOR, Ceramic Disc .001 µF 20%, 1 kV	91418	Type B	100076	3
	C14	CAPACITOR, Tant 4.7 µF 20%, 20V	56289	196D475X0035JA1	106513	1
	C15	CAPACITOR, Ceramic Disc .01 µF 100V +80-20%	91418	TA110	100103	3
	C16	Same as C15				
	C17	Same as C13				
	C18	Same as C15				
	C19	CAPACITOR, Ceramic Disc .1 µF 20%, 50V	56289	5C023104X0500C5	100178	1
	C20	Same as C13				
	C21 thru C23	CAPACITOR, Elect 5000 µF 15V	99392	23C15TS53	106459	3

REPLACEABLE PARTS LIST

TITLE 604XA LOGIC (A2) ASSEMBLY 0672520] (Cont'd)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	C24 thru C28	Same as C7				
	C29	Same as C8				
	C30	CAPACITOR, Chip .01 µF 20%, 50V	26654	17BX050S103M	106508	1
	C31 thru C35	CAPACITOR, Ceramic Disc .05 µF 10V +80-20R	71590	UK10-503	100122	5
	C36	CAPACITOR, Tant 220 µF 10%, 10V	56289	196D227X9010TA1	103497	1
	C37	Same as C2				
	C38	CAPACITOR, Dip Mica 133 pF 1%, 500V	72136	DM15FD1330FO	100323	1
	CR1 thru CR3	DIODE	03508	1N4151	100385	4
	CR4 thru CR7	DIODE, Rectifier	81483	30S05	103252	4
	CR8	Same as CR1				
	J2 thru J4	CONNECTOR, 20 Pin Header	30146	922584-20	117211	3
	J5	CONNECTOR, RF	98291	51-051-0000	101260	1
	K1	RELAY	00779	53451-1	117473	1
	L1	INDUCTOR, Bead	52542	112420	112420	1
	Q1	TRANSISTOR, SIPNP	04713	MPSH81	117263	2
	Q2	Same as Q1				
	Q3	TRANSISTOR, SINPN	52542	037592	037592	1
	Q4	TRANSISTOR, SINPN	04713	MPSA12	101396	2
	Q5	Same as Q4				
	Q6 thru Q13	TRANSISTOR, SIPNP	04713	MPSA63	117349	8

TITLE 604XA LOGIC (A2) ASSEMBLY 06725201 (Cont'd)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	R1	RESISTOR, CC 100 k 5%, 1/4W	01121	CB1045	101558	3
	R2	RESISTOR, CC 910 k 5%, 1/4W	01121	CB9145	101885	1
	R3	RESISTOR, CC 1 M 5%, 1/4W	01121	CB1055	101605	1
	R4	RESISTOR, CC 1 k 5%, 1/4W	01121	CB1025	101569	5
	R5	RESISTOR, CC 100 Ω 5%, 1/4W	01121	CB1015	101609	3
	R6	RESISTOR, CC 27 k 5%, 1/4W	01121	CB2735	101587	1
	R7	RESISTOR, CC 390 Ω 5%, 1/4W	01121	CB3915	101592	7
	R8	Same as R7				
	R9	Same as R5				
	R10	Same as R7				
	R11	Same as R7				
	R12	Same as R5				
	R13	Same as R7				
	R14	Same as R7				
	R15	RESISTOR, CC 820 Ω 5%, 1/4W	01121	CB8215	101567	1
	R16	Same as R7				
	R17	RESISTOR, CC 270 Ω 5%, 1/4W	01121	CB2715	101542	1
	R18	RESISTOR, CC 220 Ω 5%, 1/4W	01121	CB2215	101566	1
	R19	RESISTOR, CC 68 Ω 5%, 1/8W	01121	BB6805	101700	1
	R20	RESISTOR, CC 220 Ω 5%, 1/8W	01121	BB2215	101798	1
	R21	Same as R1				
	R22	RESISTOR, CC 10 k 5%, 1/4W	01121	CB1035	101570	2

TITLE 604XA LOGIC (A2) ASSEMBLY 06725201 (Cont'd)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	R23	RESISTOR, CC 560 Ω 5%, 1/8W	01121	BB5615	101710	1
	R24 thru R27	RESISTOR, CC 1 k 5%, 1/8W	01121	BB1025	101711	2
	R28	RESISTOR, CC 150 Ω 5%, 1/4W	01121	CB1515	101615	1
	R29 thru R36	RESISTOR, CC 33 k 5%, 1/4W	01121	CB3335	101576	8
	R37	RESISTOR, CC 47 k 5%, 1/4W	01121	CB4735	101574	2
	R38	Same as R37				
	R39 thru R46	RESISTOR, CC 47 Ω 5%, 1/4W	01121	CB4705	101560	8
	R47 thru R49	RESISTOR, CC 22 k 5%, 1/4W	01121	CB2235	101572	3
	R50	Same as R4				
	R51	RESISTOR, CC 470 k 5%, 1/4W	01121	CB4745	101630	1
	R52	Same as R1				
	R53	RESISTOR, CC 470 Ω 5%, 1/4W	01121	CB4715	101625	3
	R54	RESISTOR, CC 12 k 5%, 1/4W	01121	CB1235	101975	1
	R55	Same as R53				
	R56	Same as R53				
	R57	Same as R22				
	R58	Same as R4				
	R59	RESISTOR, Variable 5 k 20%, 1/2W	80294	3329H-1-502	101859	1
	R60	RESISTOR, CC 2.7 Ω 5%, 1/4W	01121	CB27G5	101784	1

REPLACEABLE PARTS LIST

TITLE 604XA LOGIC (A2) ASSEMBLY 06725201 (Cont'd)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	RN1 thru RN6	RESISTOR, Network 4 x 12 k	52542	045008	045008	6
	S1	SWITCH, 13 Pos. Push Button	52542	067284	067284	1
	U1	INTEGRATED CIRCUIT, TTL SSI Dual Pos. AND	01295	SN75451A	045290	1
	U2	INTEGRATED CIRCUIT, TTL SSI 4-IN NAND	01295	SN74LS20N	103969	1
	U3	INTEGRATED CIRCUIT, TTL SSI Triple 3-IN NAND	01295	SN74LS10N	103968	1
	U4	INTEGRATED CIRCUIT PROM	52542	055998	055998	1
	U5	INTEGRATED CIRCUIT, ECL Decade Counter	04713	MC10138P	103837	1
	U6	INTEGRATED CIRCUIT, ECL Quad ECL/TTL Translator	04713	MC10125L	045226	2
	U7	INTEGRATED CIRCUIT Counter	52542	055095	055095	1
	U8	INTEGRATED CIRCUIT, TTL BCD Counter	01295	SN74LS196N	103164	3
	U9	INTEGRATED CIRCUIT, TTL Quad 2-IN OR	01295	SN74LS32N	103972	1
	U10	INTEGRATED CIRCUIT, CMOS Hex Inverter Buffer	04713	MC14050BP	103492	1
	U11	INTEGRATED CIRCUIT, TTL BCD-7 Segment Decoder Driver	01295	SN74247N	103314	1
	U12	INTEGRATED CIRCUIT, ECL Quad 2-IN NOR	04713	MC10100P	103712	1
	U13	INTEGRATED CIRCUIT, TTL Dual D MS Flip-Flop	04713	MC10131L	045239	1
	U14	Same as U6				
	U15	INTEGRATED CIRCUIT, TTL Quad 2-IN AND	01295	SN74LS08N	103967	1
	U16	INTEGRATED CIRCUIT, TTL Quad 2-IN NAND	01295	SN74LS00N	103130	3

REPLACEABLE PARTS LIST

TITLE 604XA LOGIC (A2) ASSEMBLY 0672520] (Cont'd)						
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	U17	INTEGRATED CIRCUIT, ECL Quad TTL/ECL Translator	04713	MC10124L	045228	1
	U18	INTEGRATED CRICUIT, TTL Hex Inverter	01295	SN7416N	045230	1
	U19	INTEGRATED CIRCUIT, CMOS Dual D Flip-Flop	04713	MC14013CP	103199	1
	U20	INTEGRATED CIRCUIT, CMOS Hex Inverter Buffer	02735	CD4049BCP	103217	1
	U21	INTEGRATED CIRCUIT, TTL Dual Retrig. One-Shot	01295	SN74LS123N	103976	2
	U22	INTEGRATED CIRCUIT, LIN Timer Wide Range	18324	NE555V	045208	1
	U23	INTEGRATED CIRCUIT, CMOS Dual BCD up Counter	04713	MC14518CP	103339	3
	U24	Same as U16				
	U25	INTEGRATED CIRCUIT, CMOS 8 Channel Data Selector	04713	MC14512CP	103942	1
	U26	Same as U23				
	U27	Same as U23				
	U28	INTEGRATED CRICUIT, TTL Binary Counter	01295	SN74LS197N	103165	1
	U29	INTEGRATED CIRCUIT, ECL Quad Line Receiver	04713	MC10115L	045254	1
	U30	Same as U8				
	U31	Same as U8				
	U32	Same as U21				
	U33	Same as U16				
	U34	P/O Rear Panel				
	U36	INTEGRATED CIRCUIT Voltage Regulator	04713	MC7902CT	103944	1
	XK1	SOCKET, 16 Pin DIL	73803	C84-16-02	117041	1
	XU7	SOCKET, 40 Pin	73803	C83-40-02	117159	1
144		SCREW, 6-32 x 5/16 PHMS	96906	MS51957-27	10063205	1
145		WASHER, Flat #6	86928	5710-23-10	100662	1

REPLACEABLE PARTS LIST

TITLE 604XA LOGIC (A2) ASSEMBLY 06725201 (Cont'd)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
146		WASHER, Internal Tooth #6	96906	MS35333-71	100647	1
147		CLAMP, Cable 5/16	95987	5/16-4 NA	100717	1
193		STANDOFF, Swage 6-32 x 7/8	06540	9543B-A-0632-17	101112	1
196		CABLE, Tie	06383	SST 1.51	101115	3
197		SWAGE, Terminal	88245	2000B	100482	6
198		SWAGE, Terminal	88245	1260B	100475	6
		PC BOARD	52542	067252	067252	1

REPLACEABLE PARTS LIST

TITLE	604XA IEEE INTERFACE (A3) ASSEMBLY 06720301 REV D (Fig 7-13,7-14)					
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	C1	CAPACITOR, Ceramic Disc .05 µF 10V +80-20%	71590	UK10-503	100122	10
	C2	CAPACITOR, Dip Mica 100 pF 5%, 500V	72136	DM10FD101JO	10017301	2
	C3	Same as C2				
	C4	Same as C1				
	C5	Same as C1				
	C6	CAPACITOR, Ceramic Disc 1000 pF 20%, 1 kV	91418	Type B	100076	1
	C7	Same as C1				
	C8	CAPACITOR, Tant 47 µF 20%, 20V	56289	196D476X020LA1	106514	1
	C9	Same as C1				
	C10	CAPACITOR, Tant 22 µF 10%, 10V	56289	196D226X9010JA1	103496	1
	C11	Same as C1				
	C12	CAPACITOR, Tant 39 µF 10%, 10V	56289	150D396X9010B2	100183	2
	C13 thru C15	Same as C1				
	C16	CAPACITOR, Dip Mica 1000 pF 5%, 100V	72136	DM15FA102JO	10024301	2
	C17	CAPACITOR, Dip Mica 330 pF 5%, 500V	72136	DM15FD331JO	10027601	4
	C18	Same as C16				
	C19	Same as C17				
	C20	Same as C1				
	C21	Same as C17				
	C22	Same as C17				
	C23	CAPACITOR, Elect 5000 µF 15V	99392	23C15TS53	106459	1
	C24	Same as C12				
	C25	CAPACITOR, Tant 1 µF 10%, 35V	56289	150D105X9035A2	100082	1

REPLACEABLE PARTS LIST

TITLE 604XA IEEE INTERFACE (A3) ASSEMBLY 06720301 (Cont'd)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	C26	CAPACITOR, Ceramic Disc .01 µF 100V +80-20%	99515	DE2-224	100103	1
	CR1	DIODE, Rectifier	81483	30S05	103252	2
	CR2	Same as CR1				
	J1	CONNECTOR, 20 Pin	30146	922584-20	117211	3
	J2	Same as J1				
	J4	Same as J1				
	J6	CONNECTOR, 18 Pin	15818	D204-018	117507	1
	Q1	TRANSISTOR, SINPN	27018	PN3646	101369	1
	R1	RESISTOR, CC 12 k 5%, 1/4W	01121	CB1235	101565	3
	R2 thru R8	RESISTOR, CC 330 Ω 5%, 1/4W	01121	CB3315	101536	7
	R9	Same as R1				
	R10	Same as R1				
	R11	RESISTOR, CC 100 k 5%, 1/4W	01121	CB1045	101558	2
	R12	Same as R11				
	R13	RESISTOR, CC 22 k 5%, 1/4W	01121	CB2235	101572	9
	R14	RESISTOR, CC 47 k 5%, 1/4W	01121	CB4735	101574	1
	R15 thru R22	Same as R13				
	R23	RESISTOR, CC 6.2 k 5%, 1/4W	01121	CB6225	101608	4
	R24	RESISTOR, CC 3 k 5%, 1/4W	01121	CB3025	101548	4
	R25	Same as R23				
	R26	Same as R24				
	R27	Same as R23				
	R28	Same as R24				

REPLACEABLE PARTS LIST

TITLE 604XA IEEE INTERFACE (A3) ASSEMBLY 06720301 (Cont'd)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	R29	Same as R23				
	R30	Same as R24				
	RN1	RESISTOR, Network 4 x 12 k	52542	045008	045008	3
	RN2	Same as RN1				
	RN3	RESISTOR, Network 4 x 1.8 k	52542	067114	067114	2
	RN4	Same as RN3				
	RN5	Same as RN1				
	S1	SWITCH, 6 Pole	27264	10040-106-0-0-0	117489	1
	U1	INTEGRATED CIRCUIT, TTL Dual D Flip-Flop	01295	SN74LS74N	103132	7
	U2	INTEGRATED CRICUIT, PROM	52542	067393	067393	1
	U3	INTEGRATED CIRCUIT, TTL RAM	01295	SN7489N	103219	1
	U4	INTEGRATED CIRCUIT, PROM	52542	067394	067394	1
	U5	INTEGRATED CIRCUIT, TTL Quad 2:1 Line Mux	01295	SN74LS157N	117249	1
	U6	INTEGRATED CIRCUIT, TTL Binary Counter	01295	SN74LS197N	103165	1
	U7	INTEGRATED CIRCUIT, TTL 8-IN NAND	01295	SN74LS30N	103971	4
	U8	INTEGRATED CIRCUIT, TTL Quad 2-IN OR	01295	SN74LS32N	103973	3
	U9	Same as U1				
	U10	INTEGRATED CIRCUIT, TTL Quad 2-IN NAND	01295	SN74LS00N	103130	8
	U11	INTEGRATED CIRCUIT, CMOS Dual Mono MVB	04713	MC14528BCP	045289	1
	U12	INTEGRATED CIRCUIT, CMOS Hex Inverter Buffer	04713	MC14050BP	103492	1
	U13	INTEGRATED CIRCUIT, CMOS 8 Bit Priority Encoder	04713	MC14532BCP	116213	1
	U14	INTEGRATED CIRCUIT, TTL Quad 2-IN NAND	01295	SN74LS08N	103967	10
	U15	Same as U10				

TITLE 604XA IEEE INTERFACE (A3) ASSEMBLY 06720301 (Cont'd)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	U16	Same as U8				
	U17	INTEGRATED CIRCUIT, TTL 5 Bit Comparator	02763	93L24PC	117020	1
	U18	INTEGRATED CIRCUIT, TTL Hex Inverter	01295	SN74LS04N	103749	3
	U19	INTEGRATED CIRCUIT, TTL 4 Bus Driver/Receiver	04713	MC3446	117021	3
	U20	Same as U19				
	U21	Same as U10				
	U22	INTEGRATED CIRCUIT Dual One Shot	01295	SN74LS123N	103976	4
	U23	Same as U14				
	U24 thru U26	Same as U7				
	U27	Same as U18				
	U28	Same as U19				
	U29	Same as U14				
	U30	Same as U1				
	U31	Same as U1				
	U32	Same as U18				
	U33	Same as U14				
	U34	Same as U10				
	U35	Same as U10				
	U36	INTEGRATED CIRCUIT, TTL 4-10 Decoder/Driver	01295	SN74LS145N	103369	1
	U37	INTEGRATED CRICUIT, TTL Quad 2-IN NAND	01295	SN7426N	045252	1
	U38	Same as U10				
	U39	Same as U14				
	U40	Same as U1				
	U41	Same as U14				
	U42	Same as U10				

REPLACEABLE PARTS LIST

TITLE	604XA IEEE INTERFACE (A3) ASSEMBLY 0672030] (Cont'd)					
ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	U43	Same as U14				
	U44	INTEGRATED CIRCUIT, TTL Triple 3-IN NAND	01295	SN74LS10N	103968	1
	U45	INTEGRATED CIRCUIT, CMOS Hex Inverter Buffer	02735	CD4049	103217	1
	U46	Same as U14				
	U47	Same as U10				
	U48	Same as U14				
	U49	Same as U22				
	U50	Same as U8				
	U51	Same as U14				
	U52	Same as U1				
	U53	Same as U22				
	U54	Same as U1				
	U55	Same as U22				
	XU2 thru XU4	SOCKET, 16 Pin IC	73803	C84-16-02	117041	3
		TERMINAL, Swage	88245	2010B	100475	2
		TERMINAL, Swage	88245	2000B	100482	3
		PC BOARD	52542	067203	067203	1

REPLACEABLE PARTS LIST

TITLE 604XA DISPLAY (A4) ASSEMBLY 06722901 REV B (Fig 7-15,7-16)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	DS1 thru DS8	DISPLAY, 7 Segment LED	50522	MAN3610A	10331501	8
	DS9 thru DS19	LED, Red	50522	MV5754	103960	11
	J1	CONNECTOR, Header 20 Pin	30146	922584-20	117211	2
	J3	Same as J1				
	R1	RESISTOR, CC 47 Ω5%, 1/4W	01121	CB4705	101560	1
	R2	RESISTOR, CC 330 Ω 5%, 1/4W	01121	CB3315	101536	2
	R3	Same as R2				
	R4	RESISTOR, CC 220 Ω 5%, 1/4W	01121	CB2215	101566	1
	XDS1 thru XDS8	SOCKET, IC 14 Pin	73803	C83-14-02	117040	8
		PC BOARD	52542	067229	067229	1
		SPACER, Nylon 3/16 long	06540	9208N-115	101077	11

REPLACEABLE PARTS LIST

TITLE 604XA OSCILLATOR ASSEMBLY 05746802 REV A_1 (Fig 7-17,7-18)

ITEM	REF	COMPONENT DESCRIPTION	MFR'S CODE	MANUFACTURER'S PART NUMBER	SD STOCK NUMBER	T/Q
	C1	CAPACITOR, Variable 9-35 pF	72982	538-006D9.0-35	100159	1
	C2	CAPACITOR, Variable 15-60 pF	72982	538-011F15-60	100234	1
	C3	CAPACITOR, Dip Mica 68 pF 5%, 500V	72136	DM15ED680JO	10023901	2
	C4	CAPACITOR, Dip Mica 100 pF 5%, 500V	72136	DM15FD101JO	10017301	1
	C5	CAPACITOR, Dip Mica 47 pF 5%, 500V	72136	DM15ED470JO	10017101	1
	C6	CAPACITOR, Dip Mica 33 pF 5%, 500V	72136	DM15ED330JO	10017501	1
	C7	Same as C3				
	C8	CAPACITOR, Ceramic Disc .05 µF 10V +80-20%	71590	UK10-503	100122	1
	Q1 thru Q3	TRANSISTOR, SINPN	07263	PN4275-18	102716	3
	R1	RESISTOR, CC 1 k 5%, 1/4W	01121	CB1025	101569	2
	R2	RESISTOR, CC 33 k 5%, 1/4W	01121	CB3335	101576	1
	R3	RESISTOR, CC 3.9 k 5%, 1/4W	01121	CB3925	101601	1
	R4	RESISTOR, CC 4.7 k 5%, 1/4W	01121	CB4725	101598	1
	R5	RESISTOR, CC 3.3 k 5%, 1/4W	01121	CB3325	101559	2
	R6	Same as R1				
	R7	Same as R5				
	R8	RESISTOR, CC 470 Ω 5%, 1/4W	01121	CB4715	101625	1
	Y1	CRYSTAL 10.0 MHz	52542	039483	049483	
		TERMINAL	88245	2000B	100482	3
		SPACER, 4-40 x 1/8 Swage	71279	1300-9	100492	2
		PC BOARD	52542	057468	057468	1

CHAPTER 7
DRAWINGS

7.1 INTRODUCTION

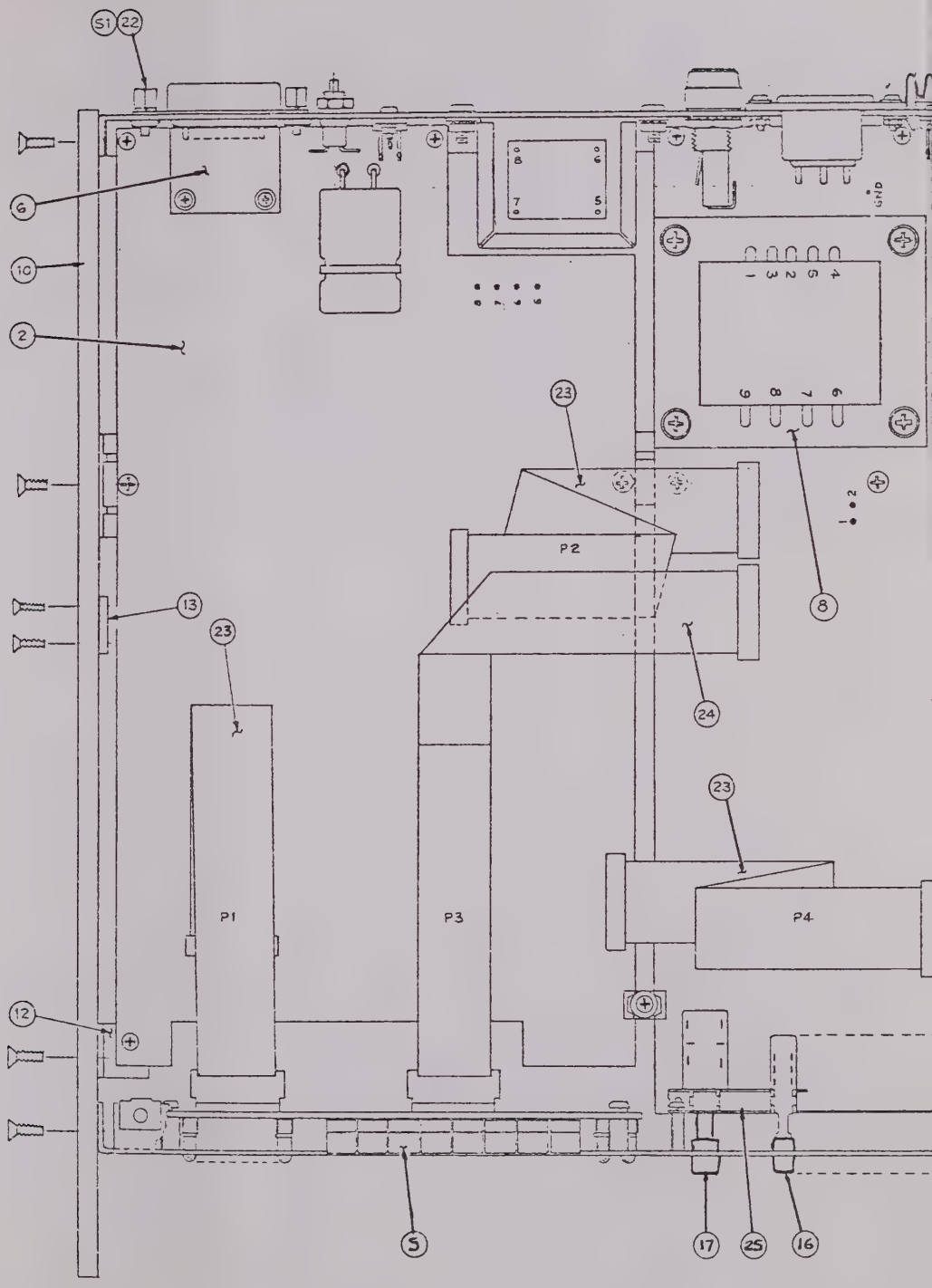
This chapter contains assembly and schematic drawings for the 6041A/6042A/6043A Frequency Counters. Each assembly drawing and its corresponding schematic diagram appear on facing pages.

Assembly drawing callouts X and circuit reference numbers (R6,Q18, ets.) are defined in the Replaceable Parts List in Chapter 6.

Circuit descriptions for each of the schematic diagrams are included in Chapter 4, Principles of Operation. Integrated Circuit (IC) types are tabulated on each schematic.

TABLE 7-1 LIST OF SCHEMATIC AND COMPONENT LOCATION DIAGRAMS

FIG. NO.	TITLE	DRAWING NUMBER	PAGE NO.
7-1	Universal Chassis Assembly (Sheet 1 of 2)	67486	7-3
7-1	Universal Chassis Assembly (Sheet 2 of 2)	67486	7-4
7-2	Rear Panel Assembly	67395	7-5
7-3	Test Assembly 6041A	67668	7-6
7-4	Test Assembly 6042A	67287	7-7
7-5	Test Assembly 6043A	67288	7-8
7-6	Interconnect Block Diagram	67669, 67670, 67671	7-9
7-7	512 MHz Prescaler (A1) Assembly 6042A	6729901	7-10
7-8	512 MHz Prescaler (A1) Schematic 6042A	6729901	7-11
7-9	1.25 GHz Prescaler (A1) Assembly 6043A	6725001	7-12
7-10	1.25 GHz Prescaler (A1) Schematic 6043A	6725001	7-13
7-11	Logic (A2) Assembly	6725201	7-14
7-12	Logic (A2) Schematic	6725201	7-15
7-13	IEEE-488 Interface (A3) Assembly	6720301	7-16
7-14	IEEE-488 Interface (A3) Schematic	6720301	7-17
7-15	Display (A4) Assembly	6722901	7-18
7-16	Display (A4) Schematic	6722901	7-19
7-17	Oscillator Assembly	5746802	7-20
7-18	Oscillator Schematic	5746802	7-20


51
22
6
10
2
23
13
23
12
P1
P3
P2
P4
8
24
23
5
17
25
16

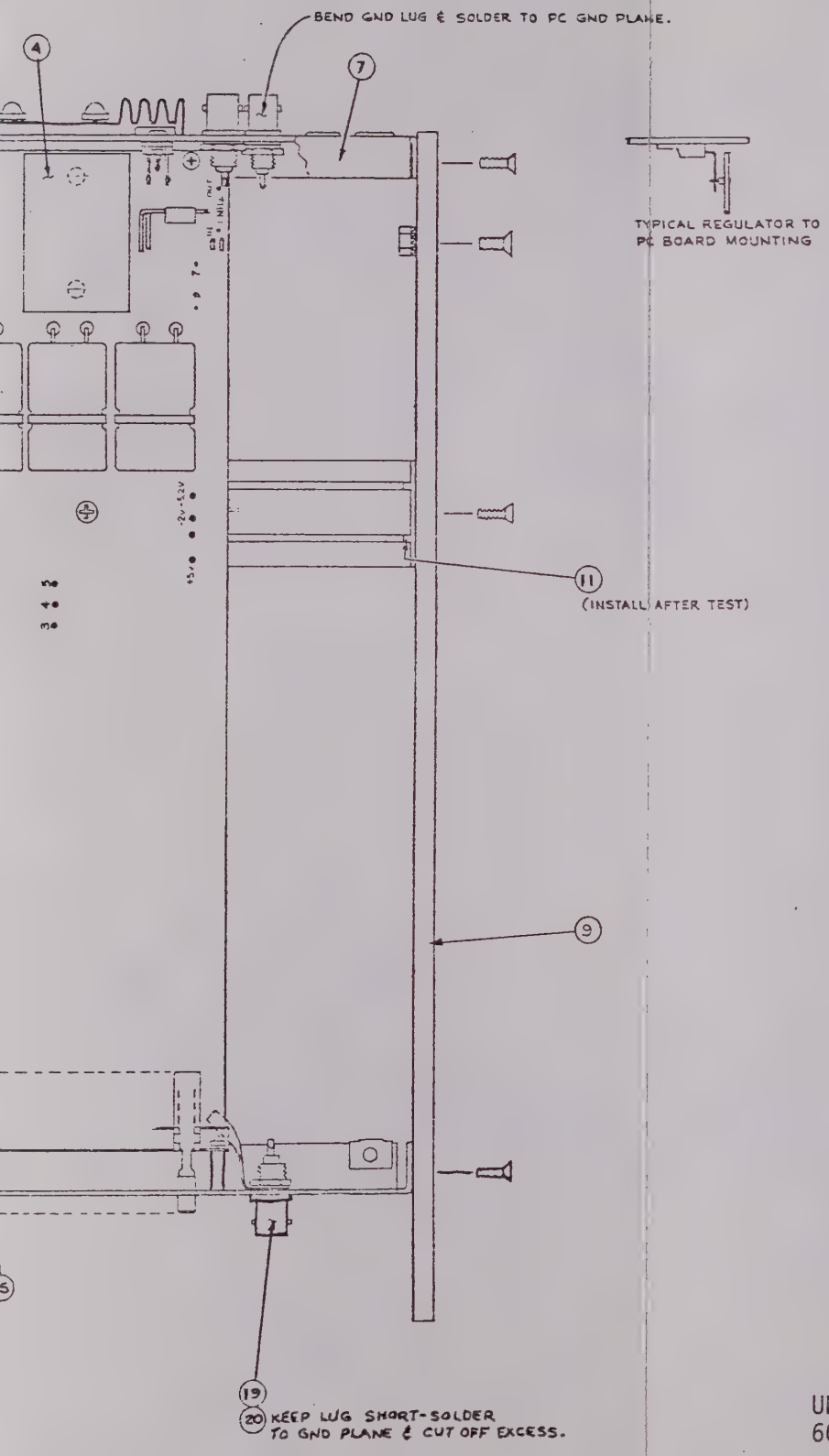
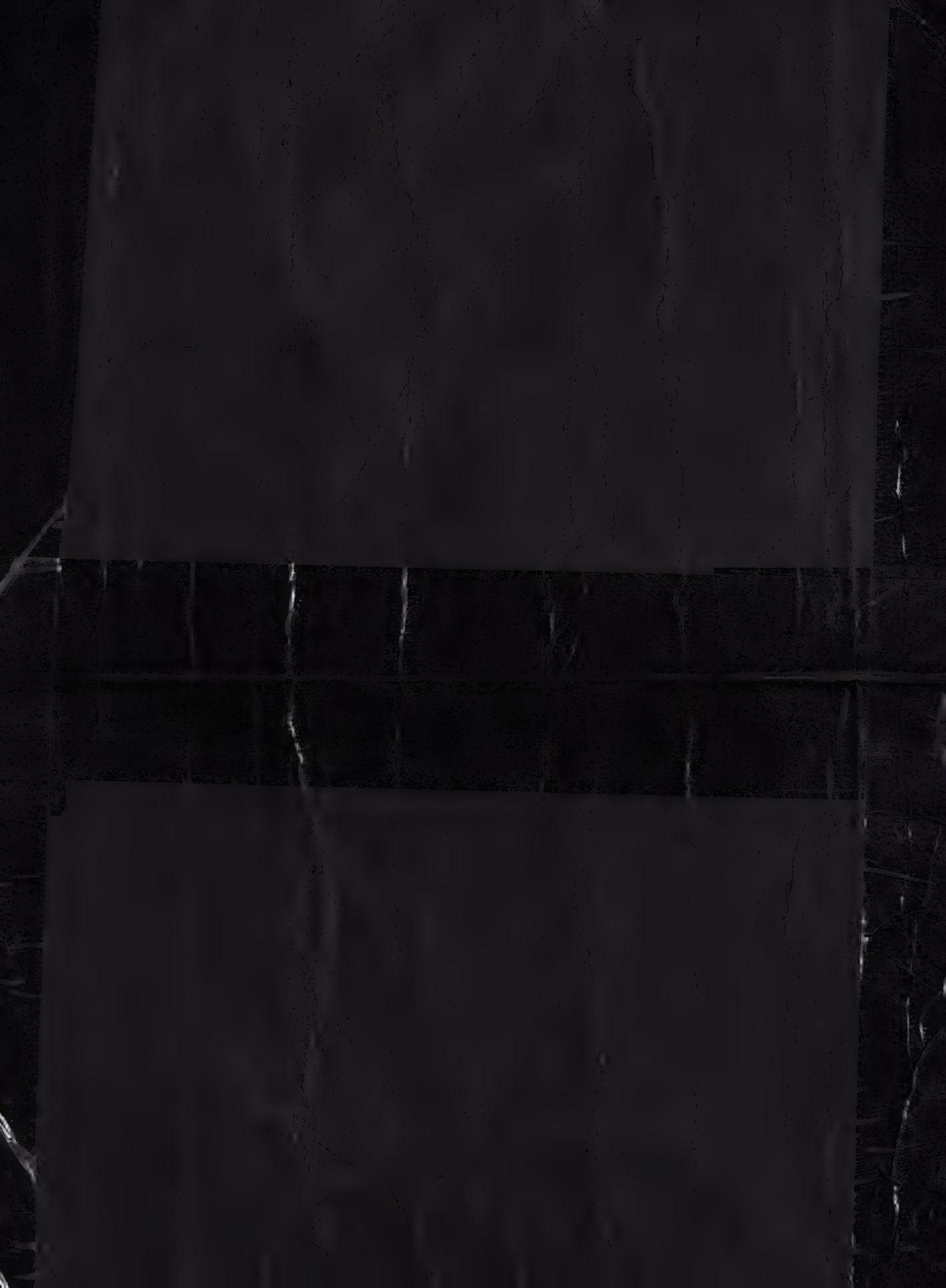
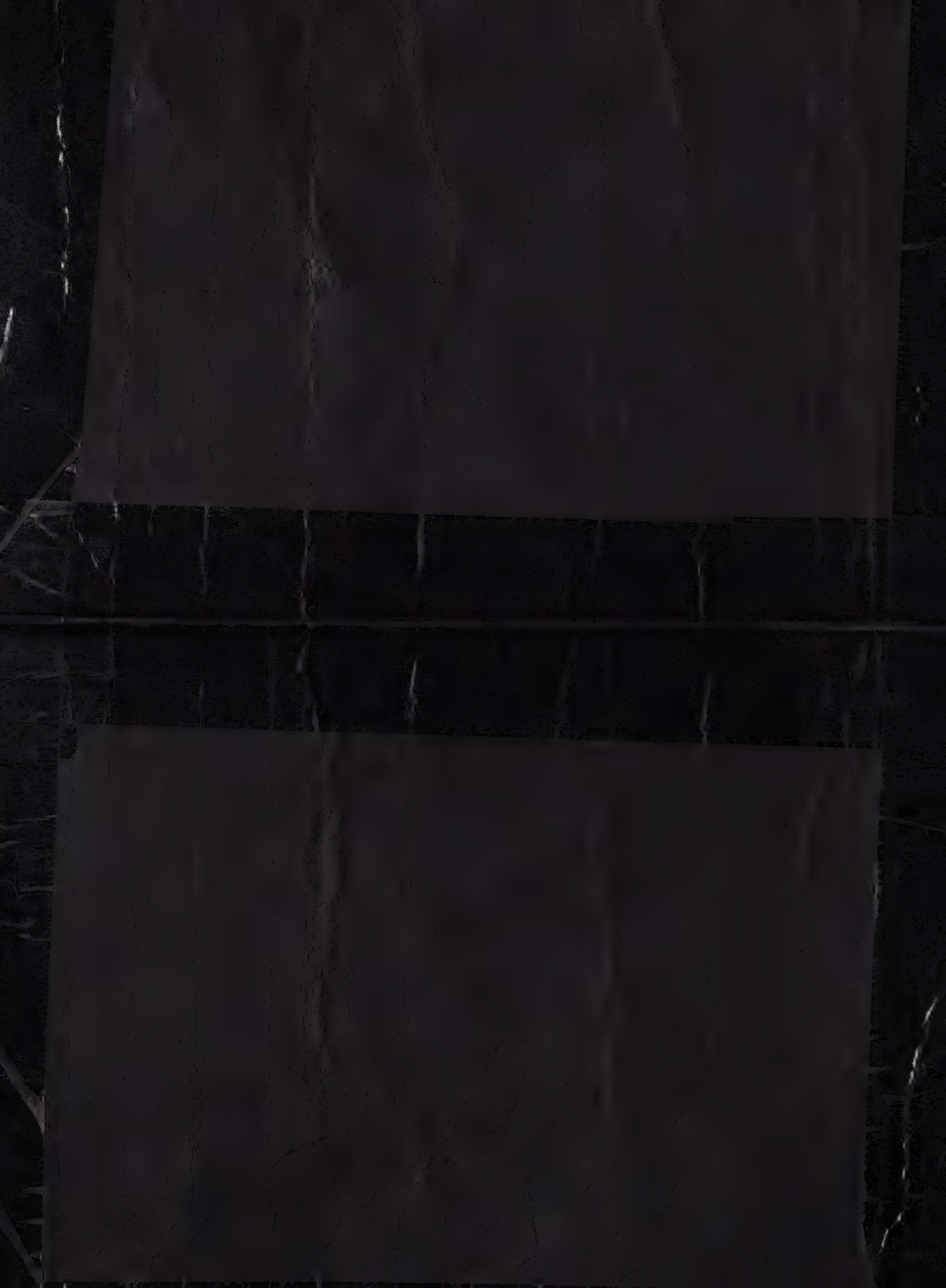
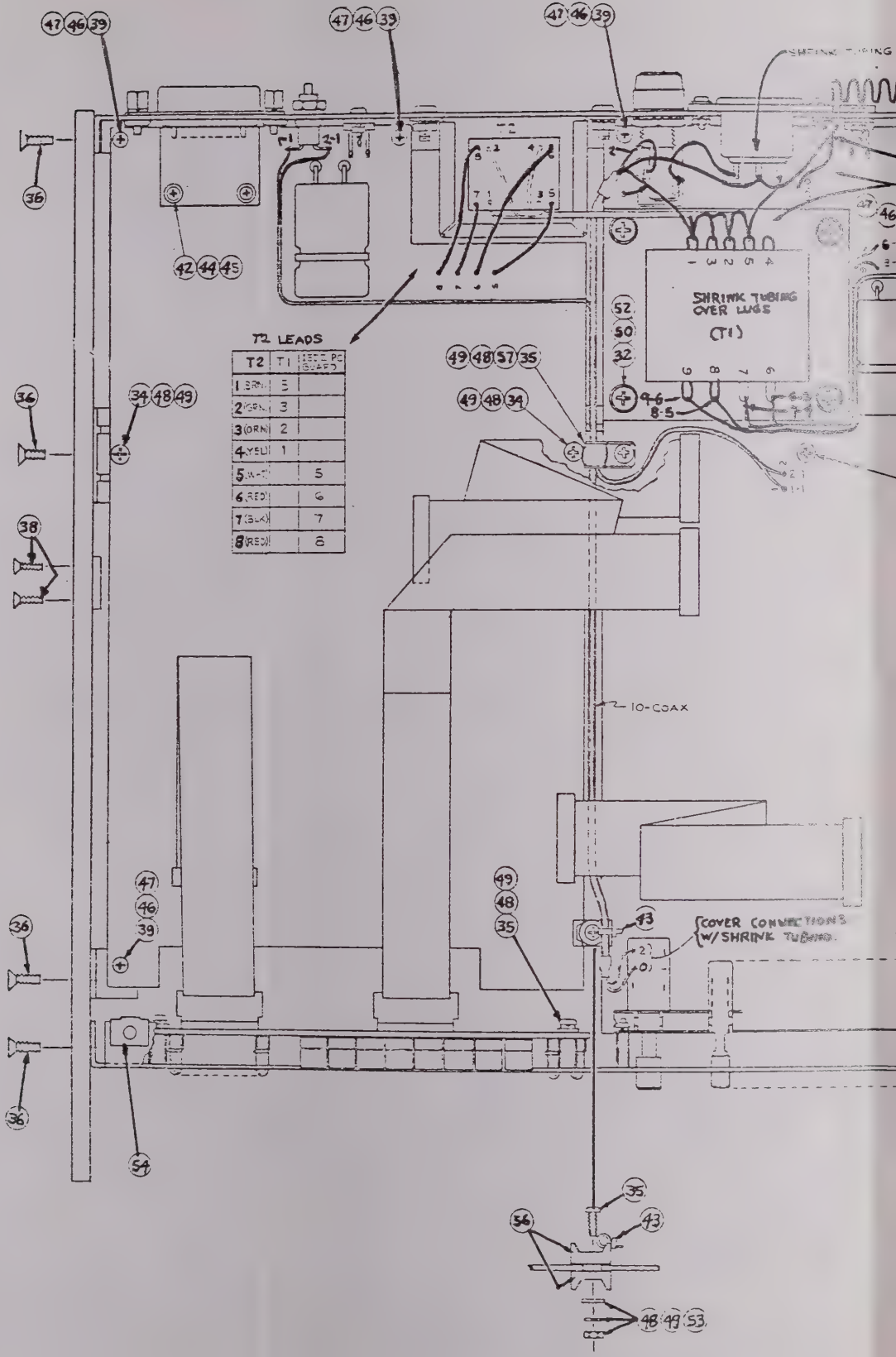
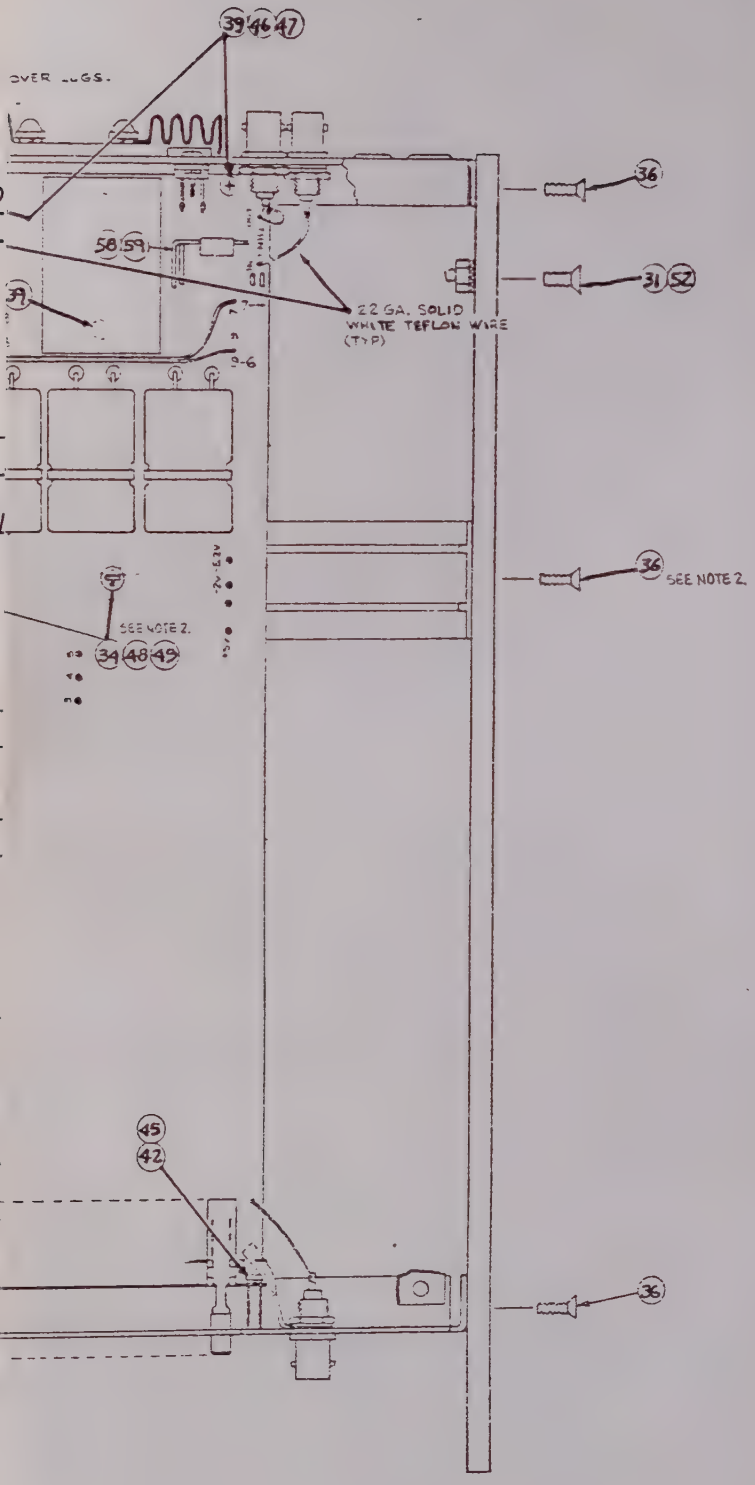


FIGURE 7-1
UNIVERSAL CHASSIS ASSEMBLY
604X Series (Sheet 1 of 2)
#67486 Rev B



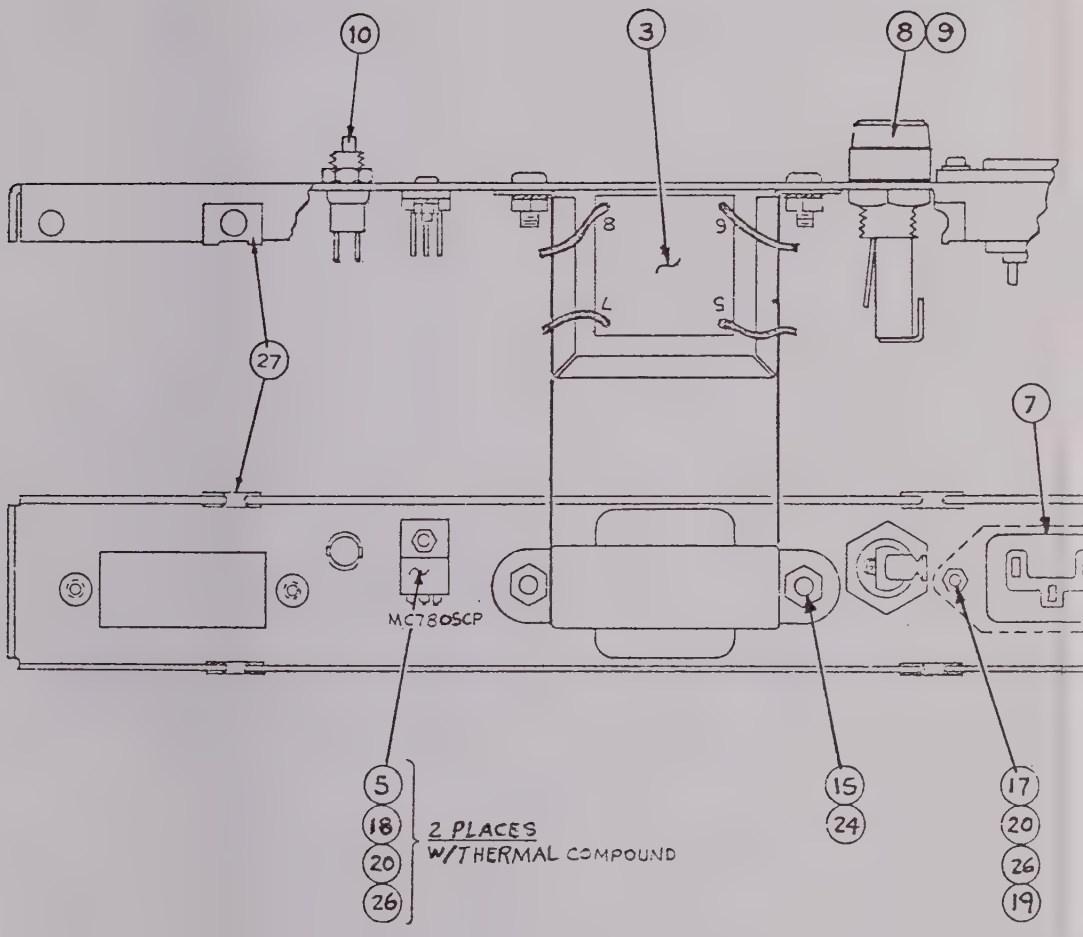



T2 LEADS
T2 | T1 | FEED PC BOARD
1 (BRN) | 5
2 (GRN) | 3
3 (ORN) | 2
4 (YELL) | 1
5 (WHT) | 5
6 (RED) | 6
7 (BLK) | 7
8 (RED) | 8
SHRINK TUBING OVER LUGS (T1)
10-COAX
COVER CONNECTIONS W/ SHRINK TUBING.



NOTE:
1) T1 & T2 HOOKED UP FOR 115VAC OPERATION. FOR 230VAC, REMOVE T1 JUMPERS 1 TO 3 & 2 TO 5. ADD T1 JUMPER 2 TO 3.

FIGURE 7-1
UNIVERSAL CHASSIS ASSEMBLY
604X Series (Sheet 2 of 2)
#67486 Rev B


10
3
8
9
8
9
L
S
27
7
MC780SCP
5
18
20
26
2 PLACES
W/THERMAL COMPOUND
15
24
17
20
26
19

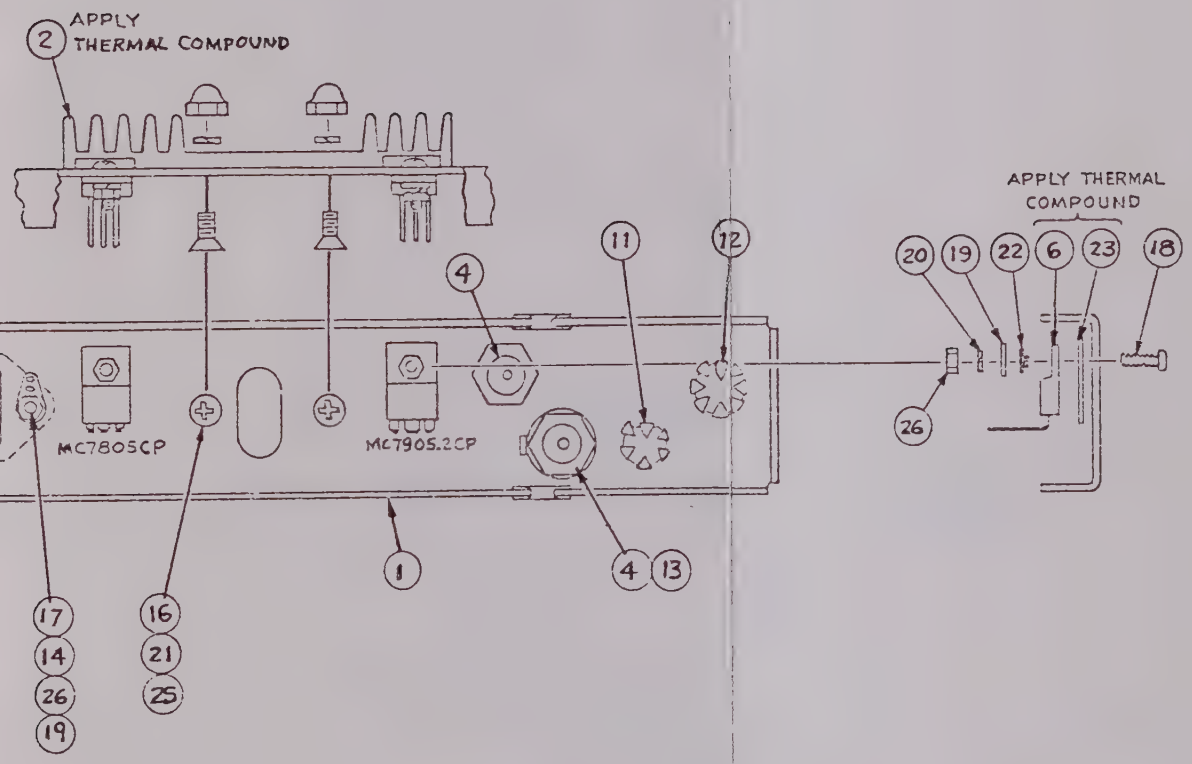
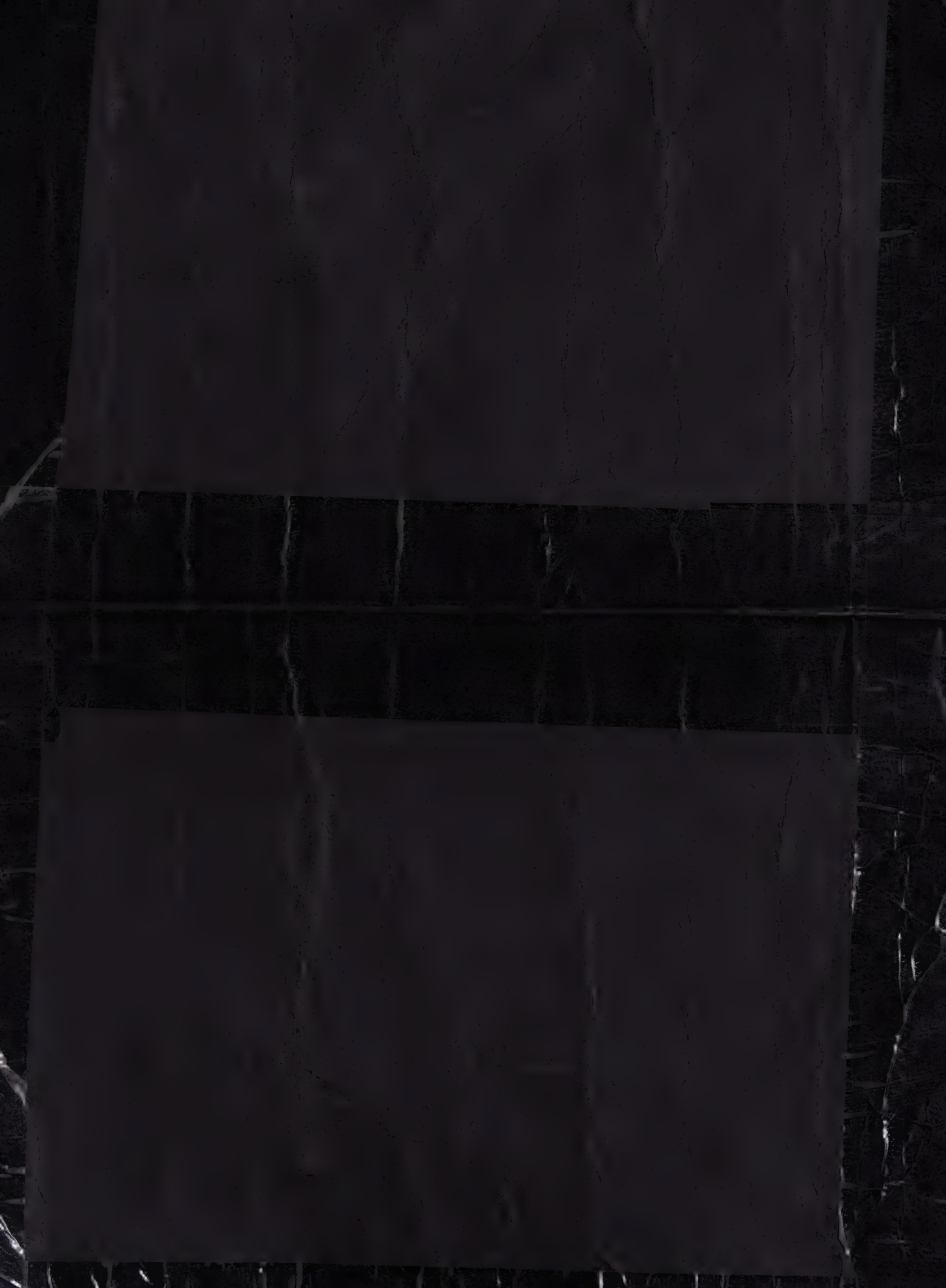
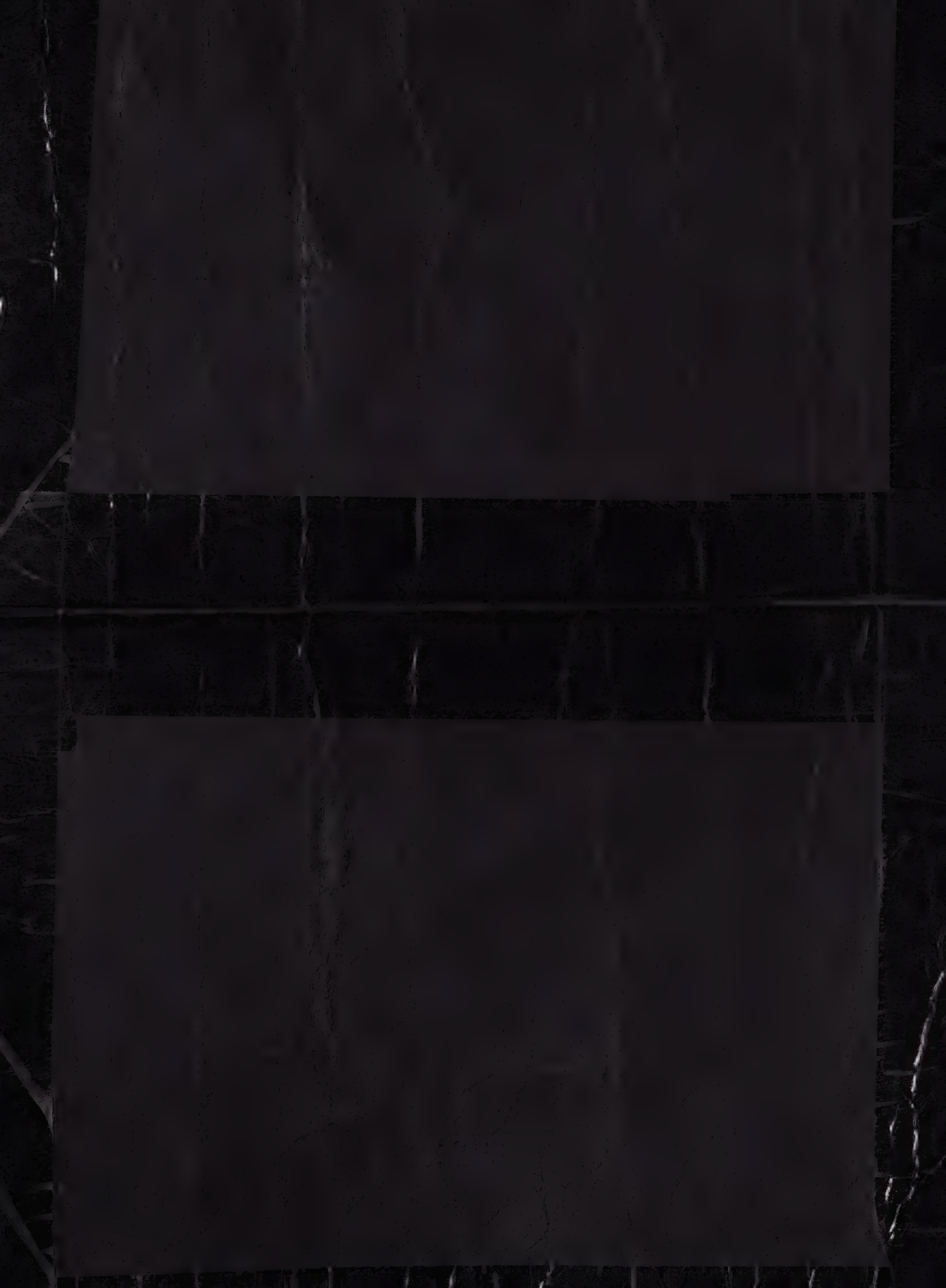
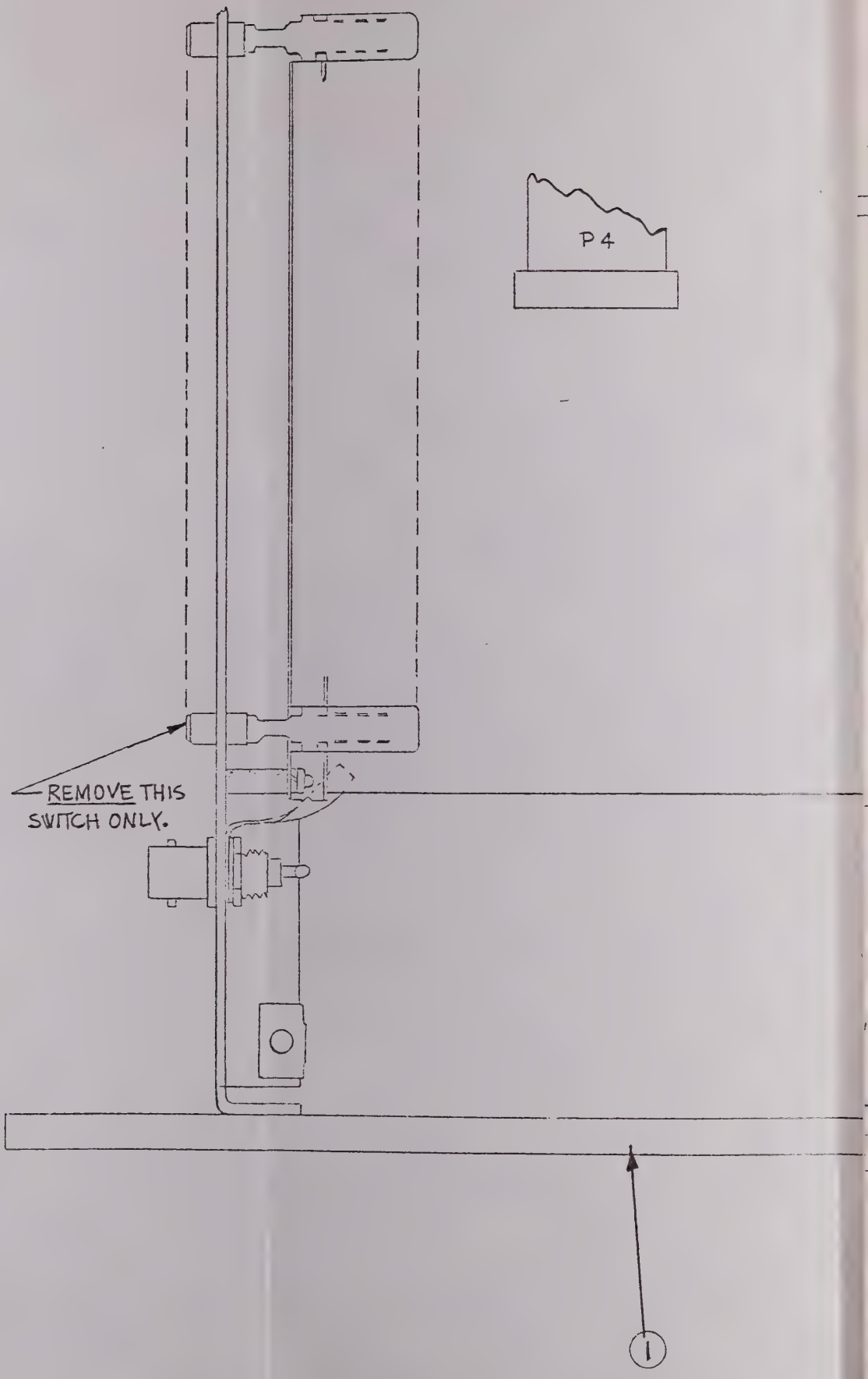


FIGURE 7-2
REAR PANEL ASSEMBLY
604X Series #67395 Rev A






P4
REMOVE THIS
SWITCH ONLY.
1

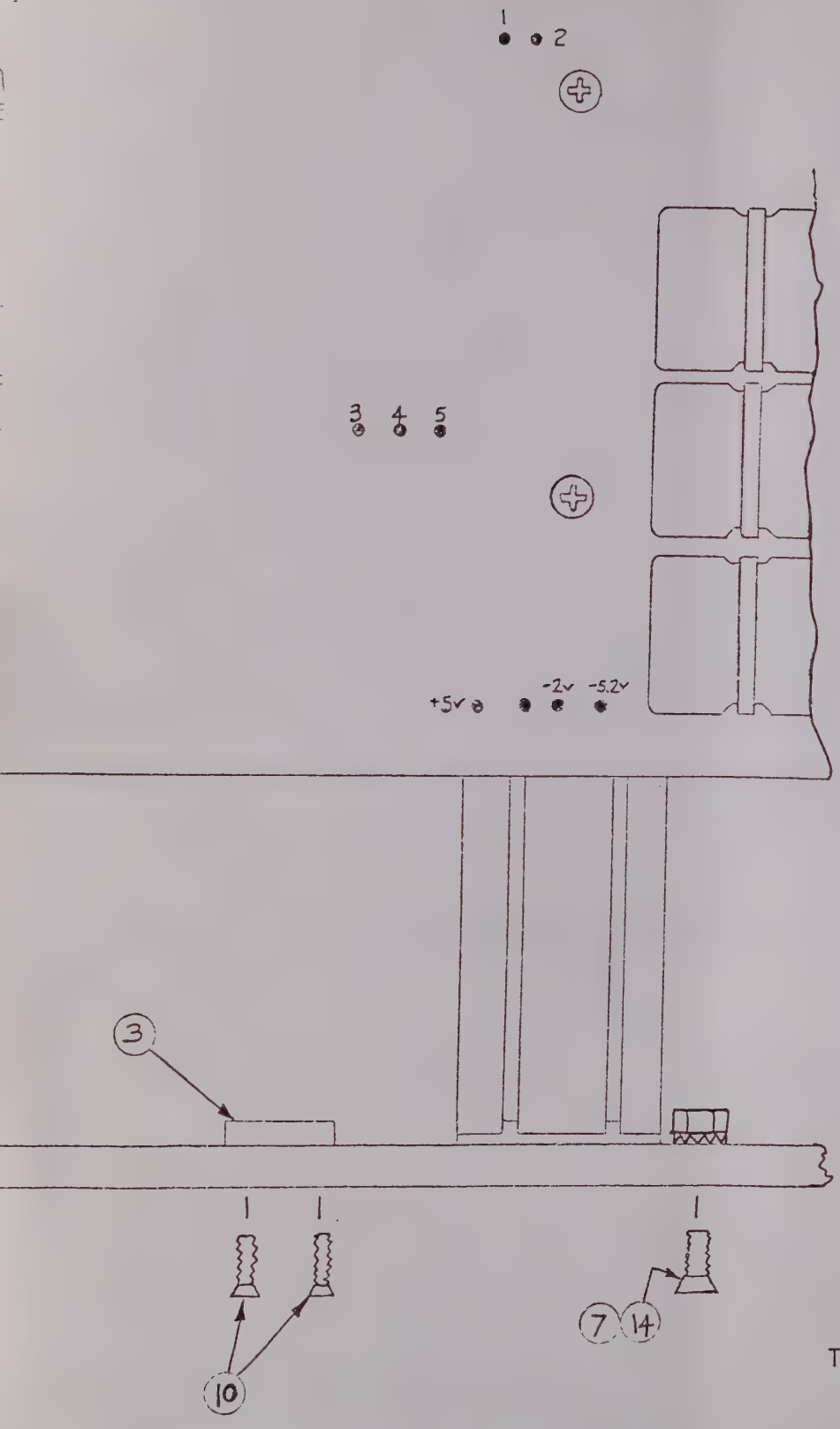
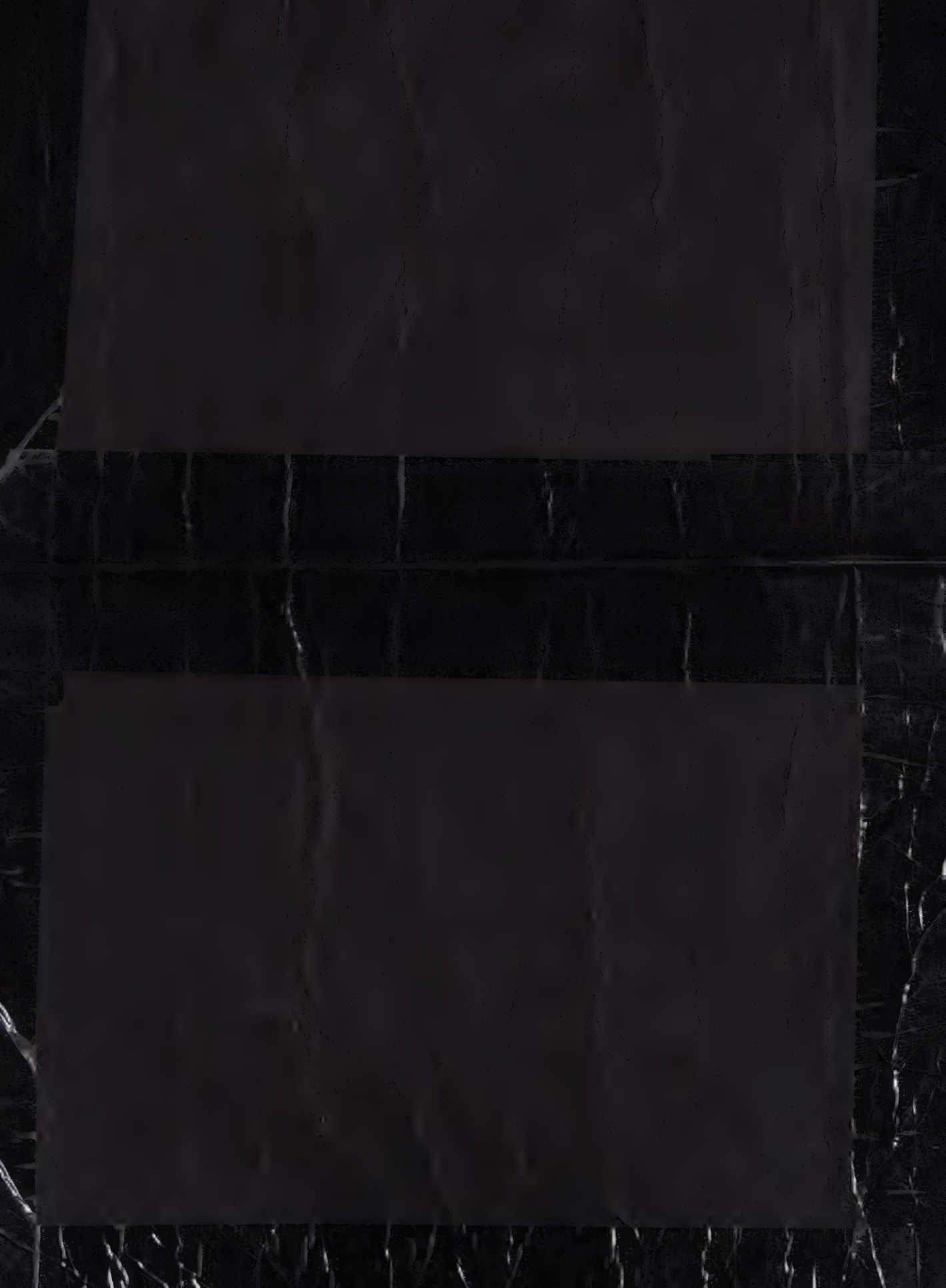
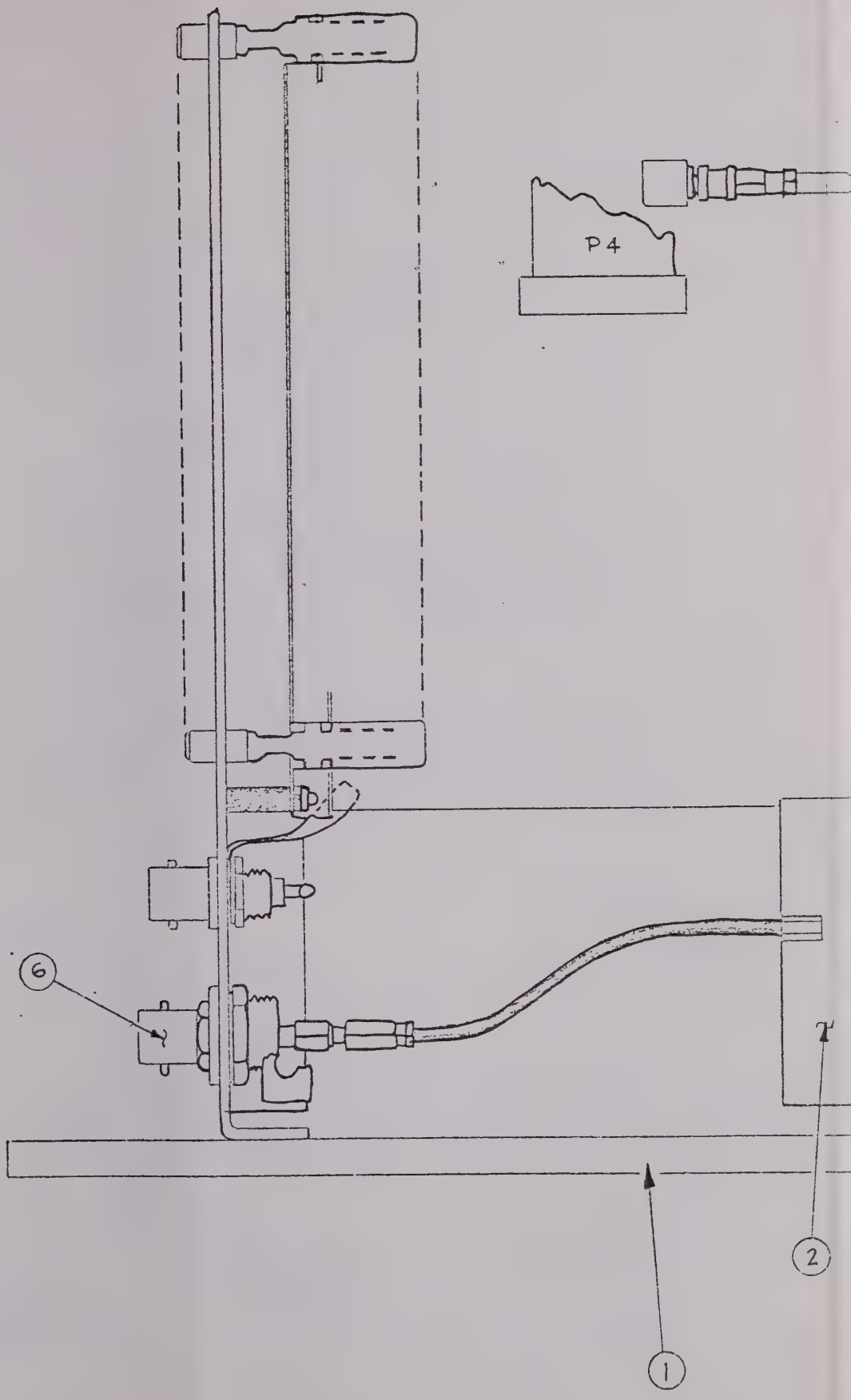


FIGURE 7-3
TEST ASSEMBLY 6041A
#67668 Rev A





604XA-2-80

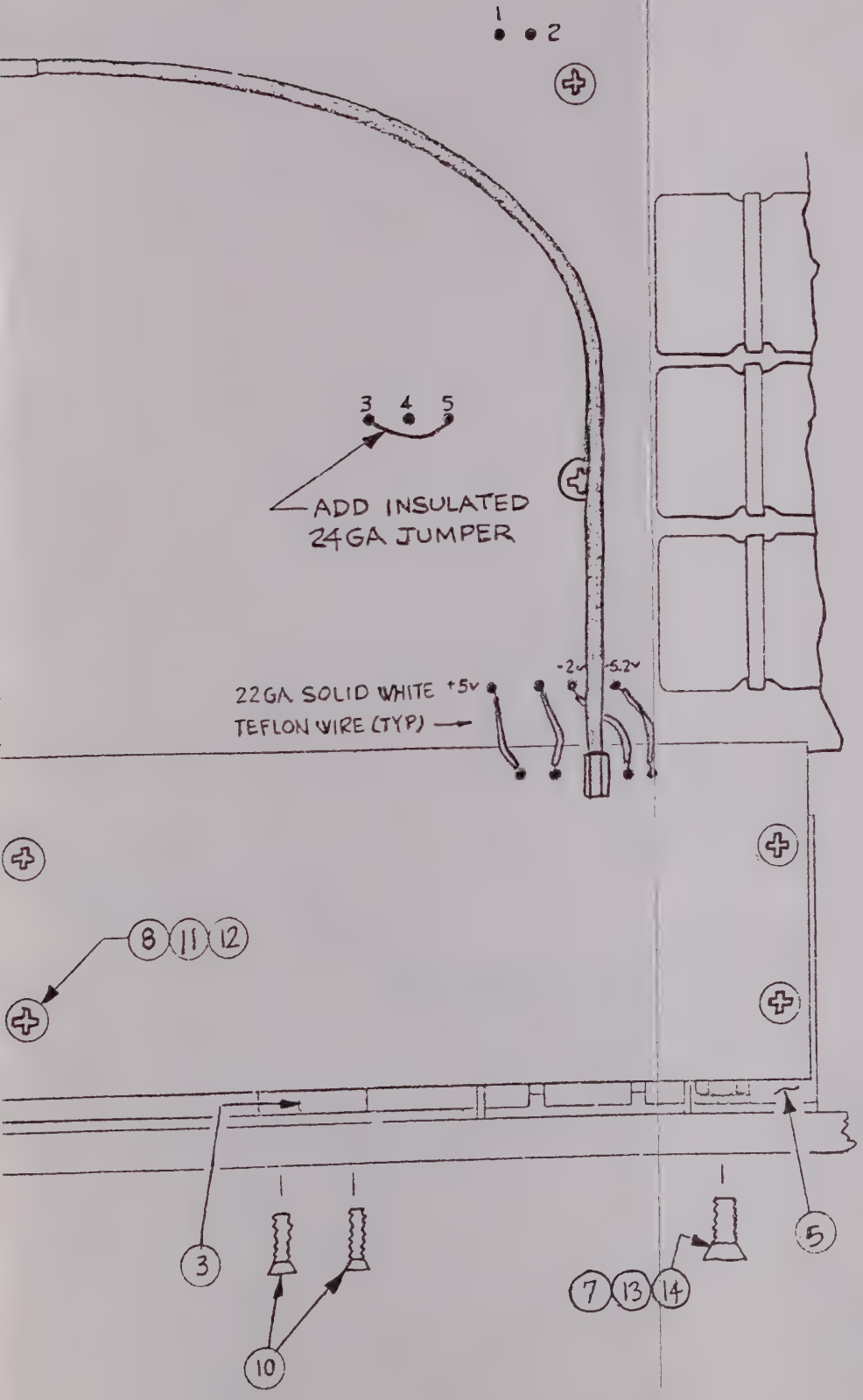
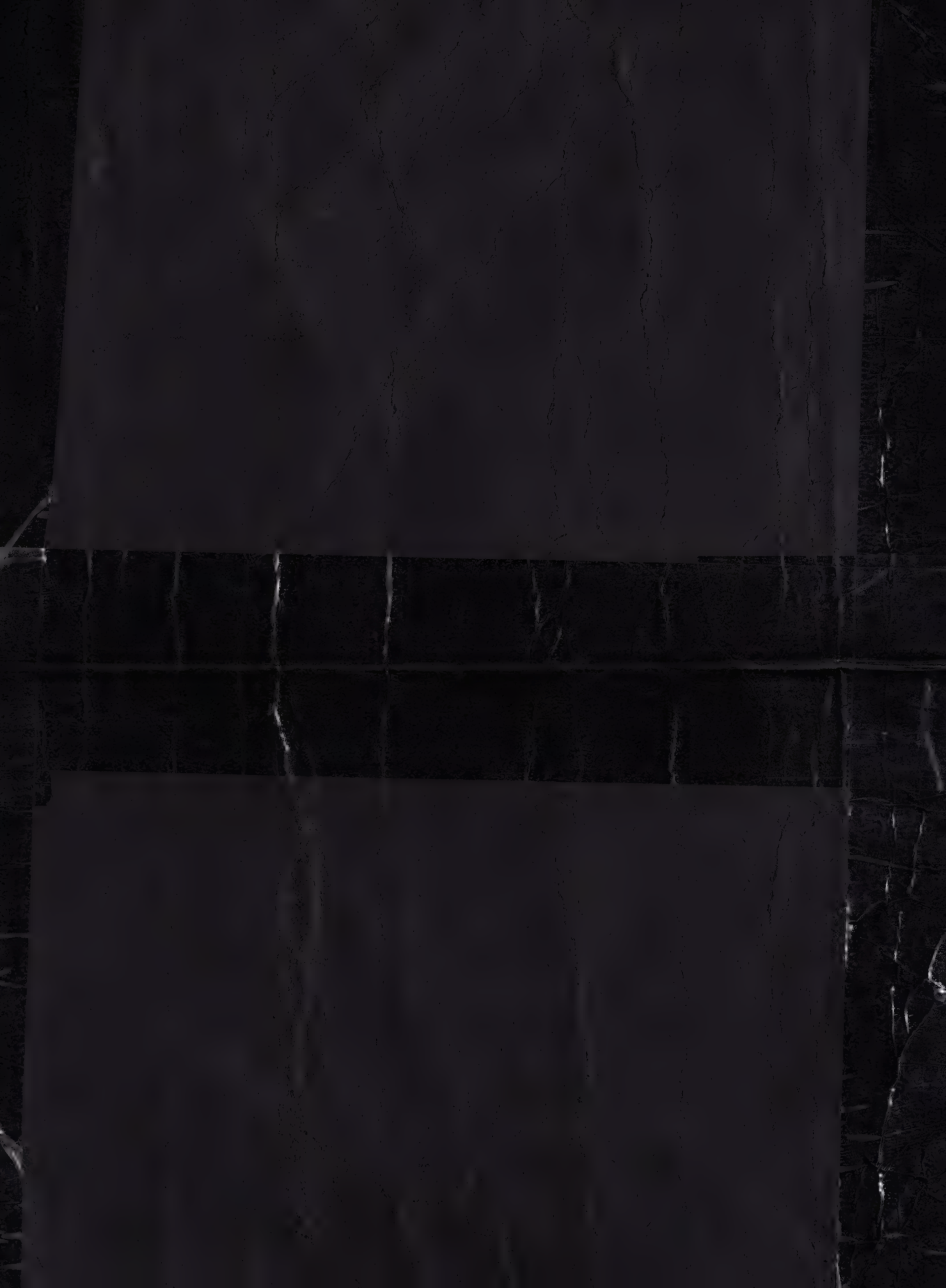
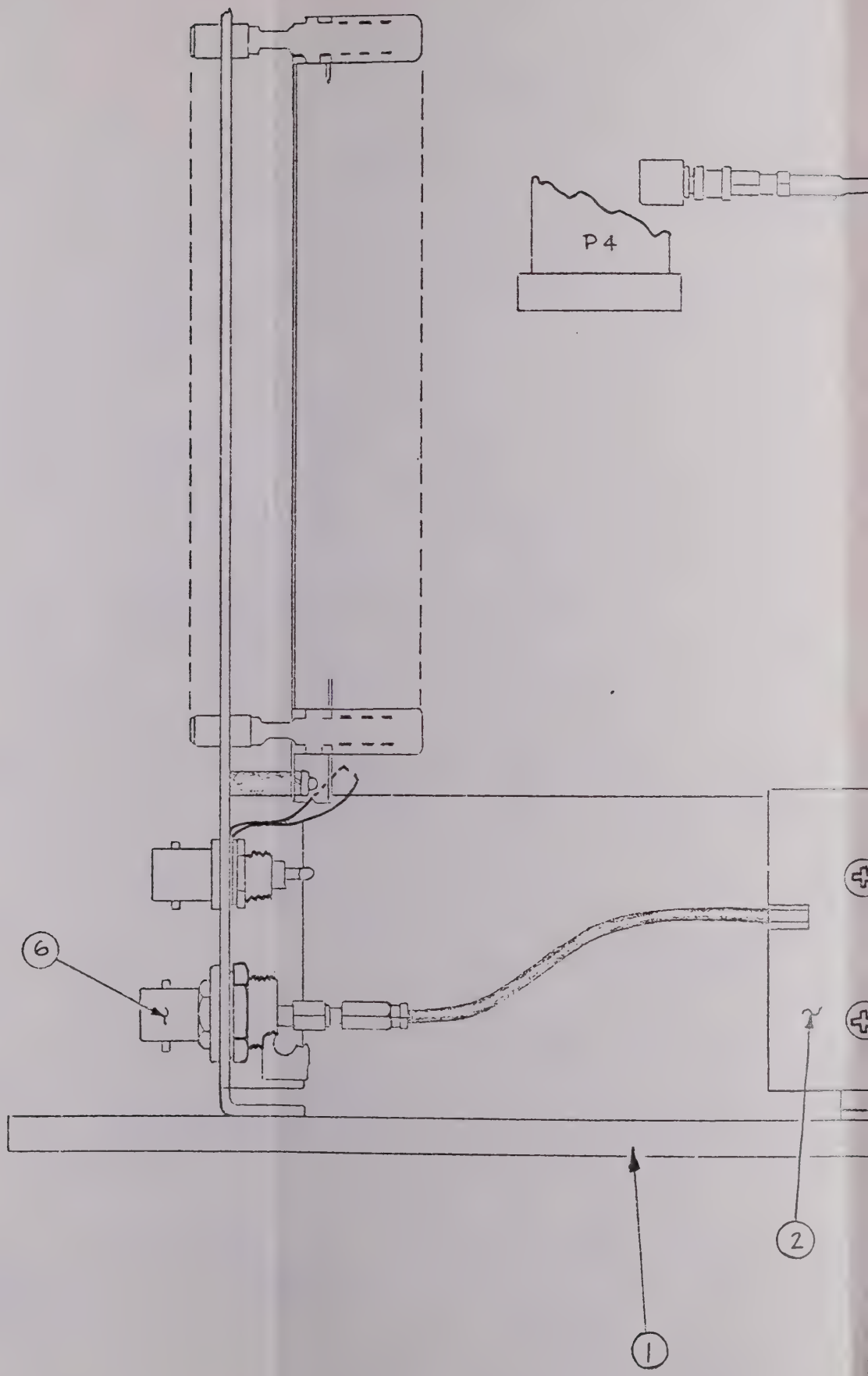


FIGURE 7-4
TEST ASSEMBLY 6042A
#67287 Rev A




P4
6
2
1

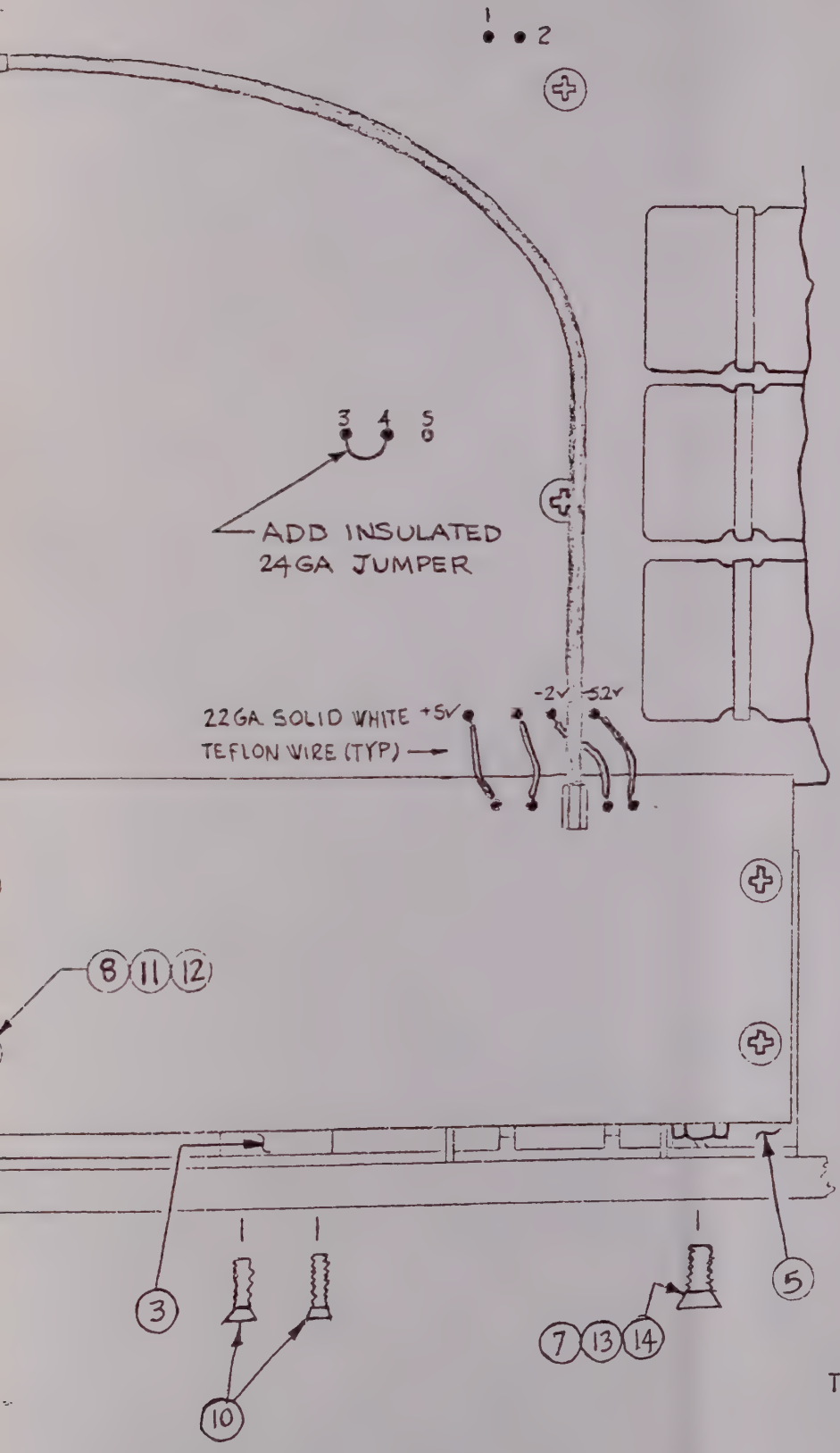


FIGURE 7-5
TEST ASSEMBLY 6043A
#67288 Rev A

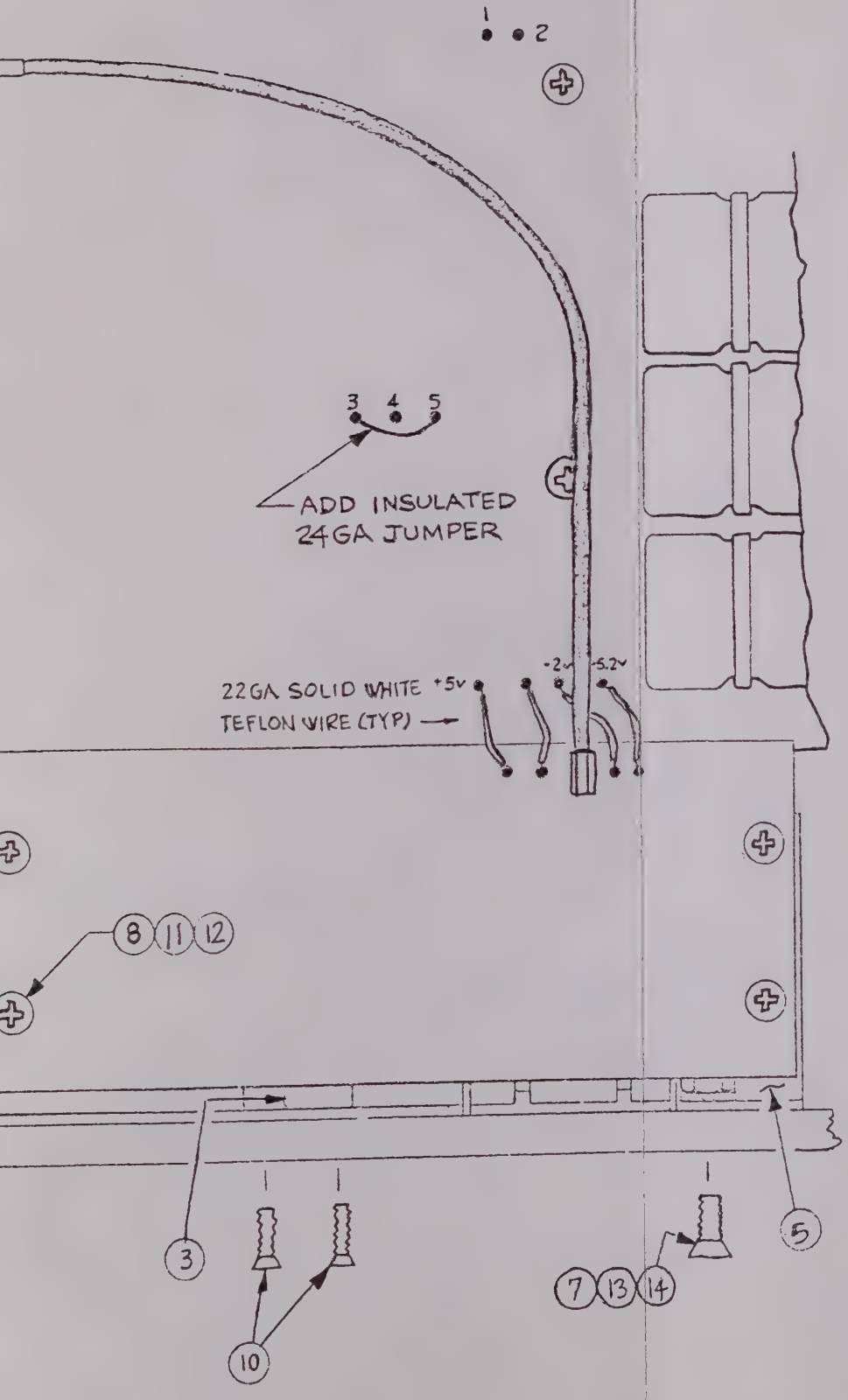
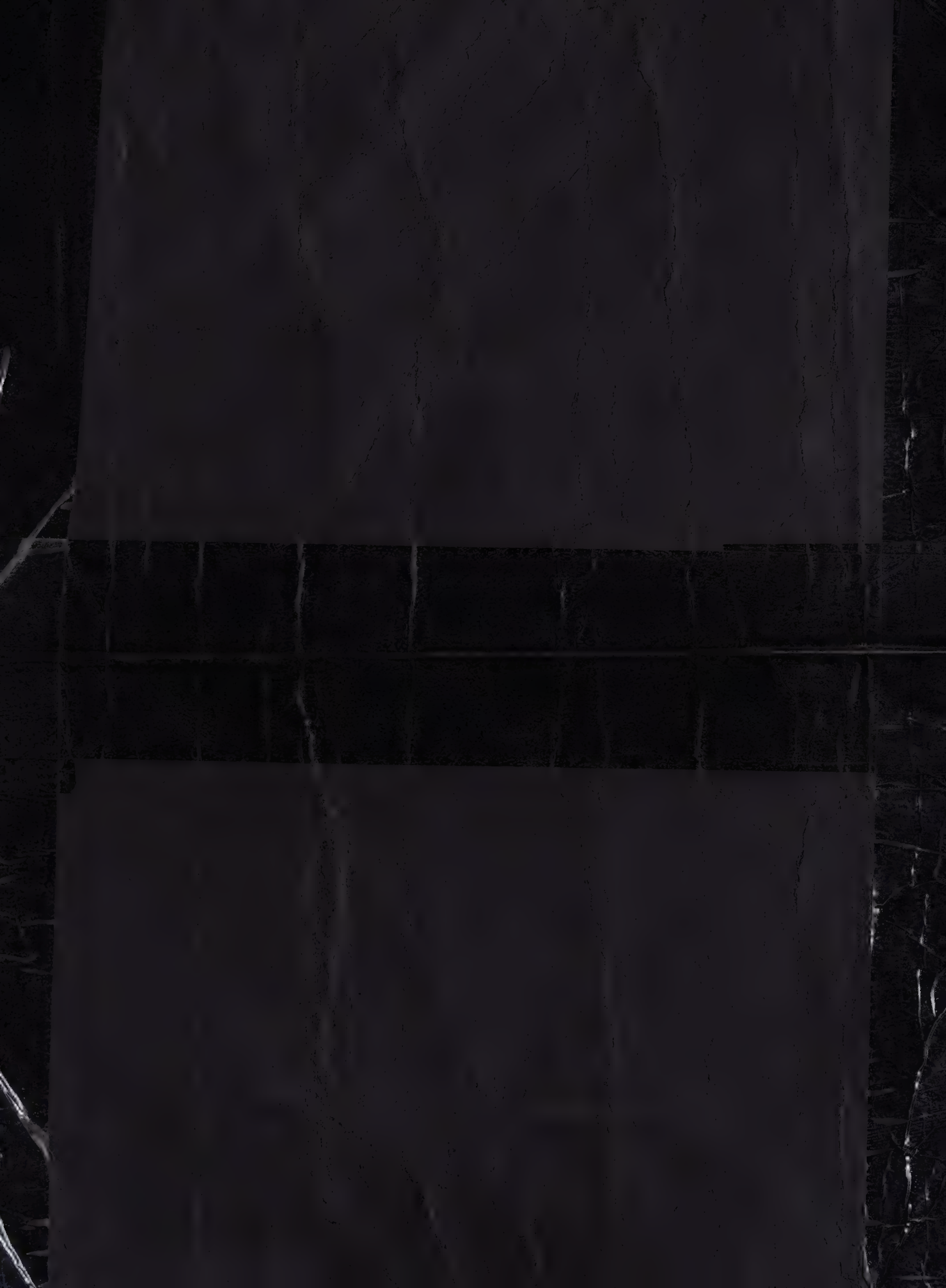
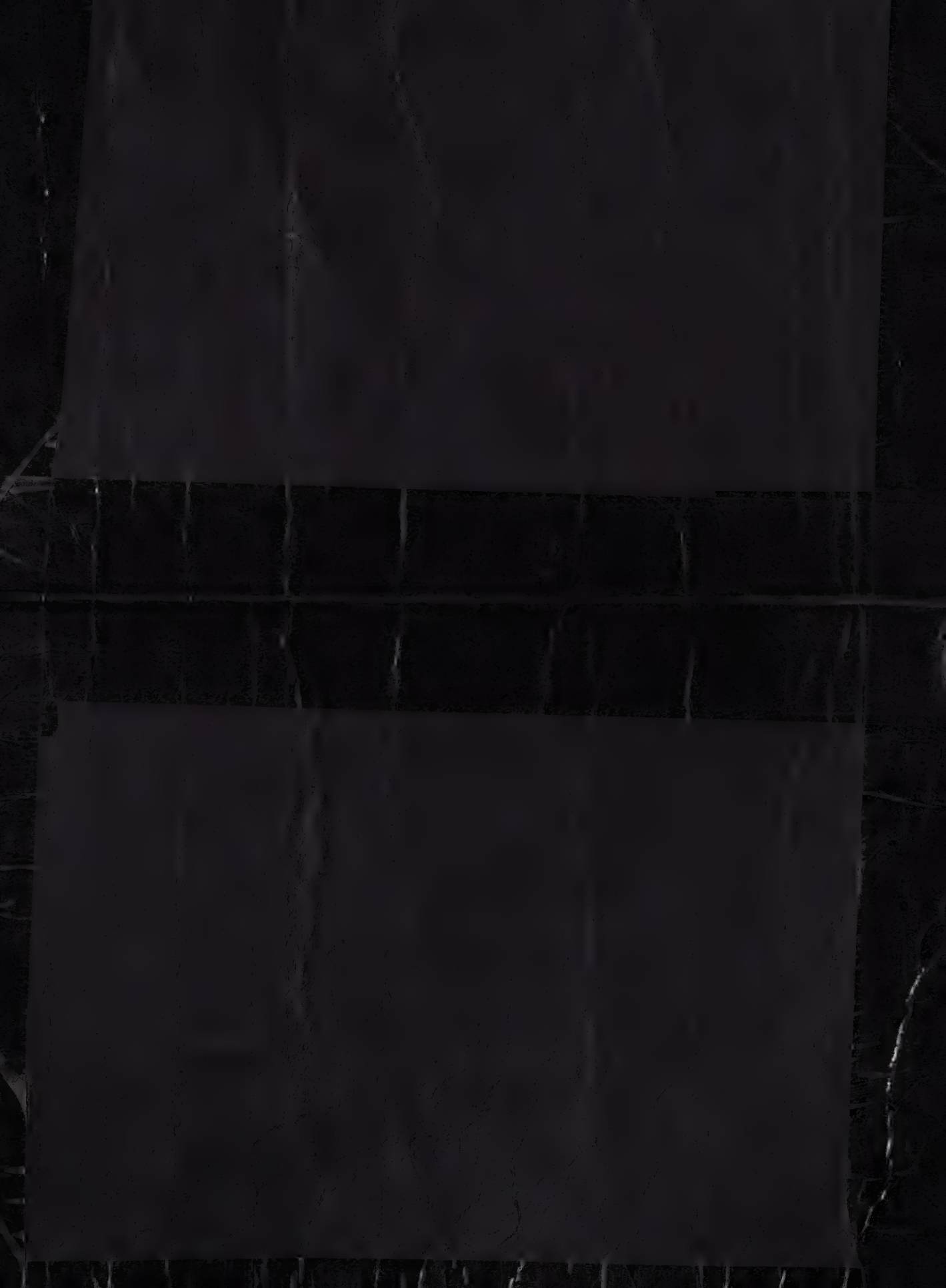
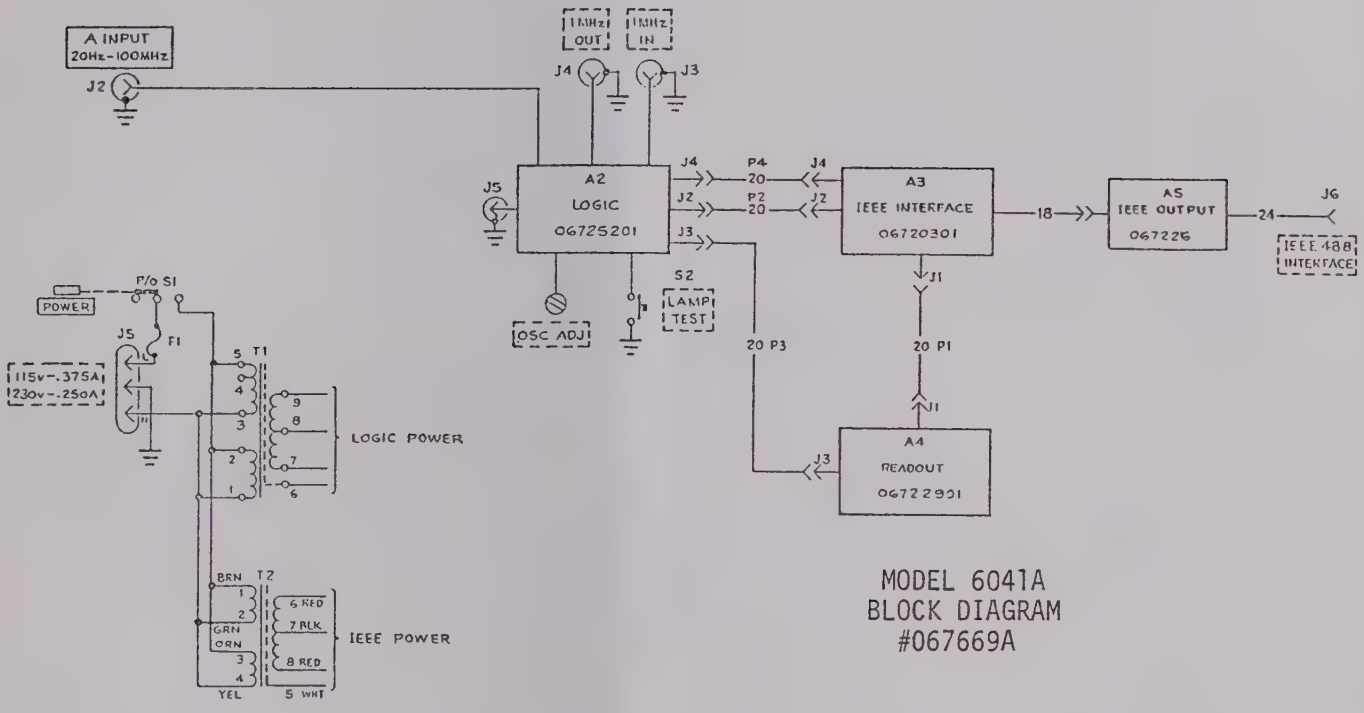


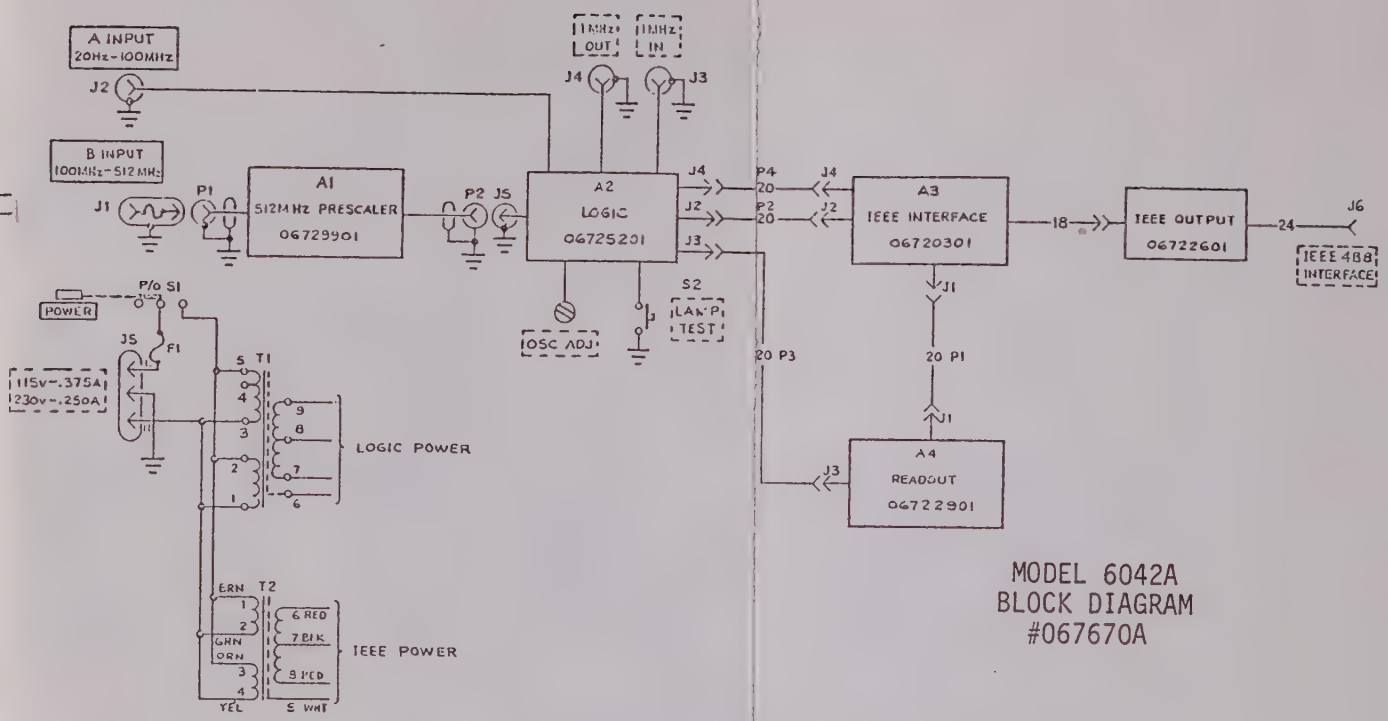
FIGURE 7-4
TEST ASSEMBLY 6042A
#67287 Rev A



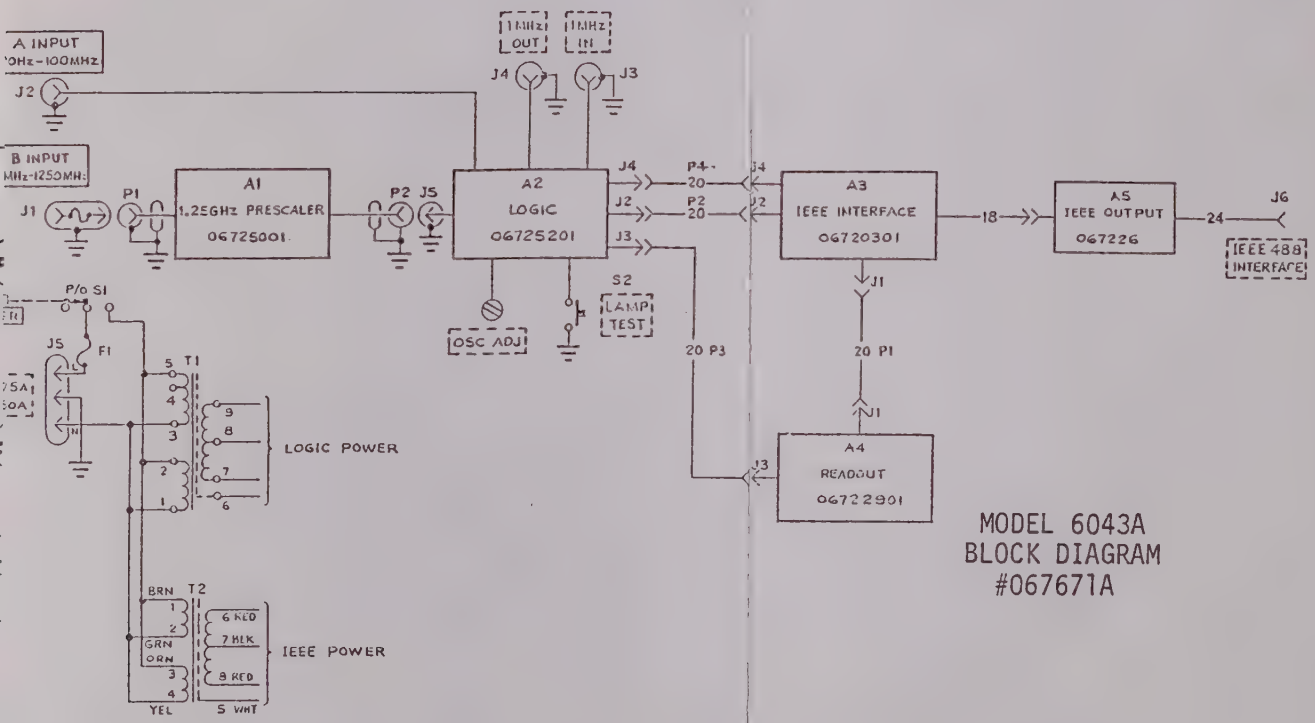




MODEL 6041A
BLOCK DIAGRAM
#067669A



MODEL 6042A
BLOCK DIAGRAM
#067670A



MODEL 6043A
BLOCK DIAGRAM
#067671A

FIGURE 7-6
INTERCONNECT BLOCK DIAGRAM
604X Series #67669/70/71 Rev A

CIRCUIT SIDE (FULL SCALE)

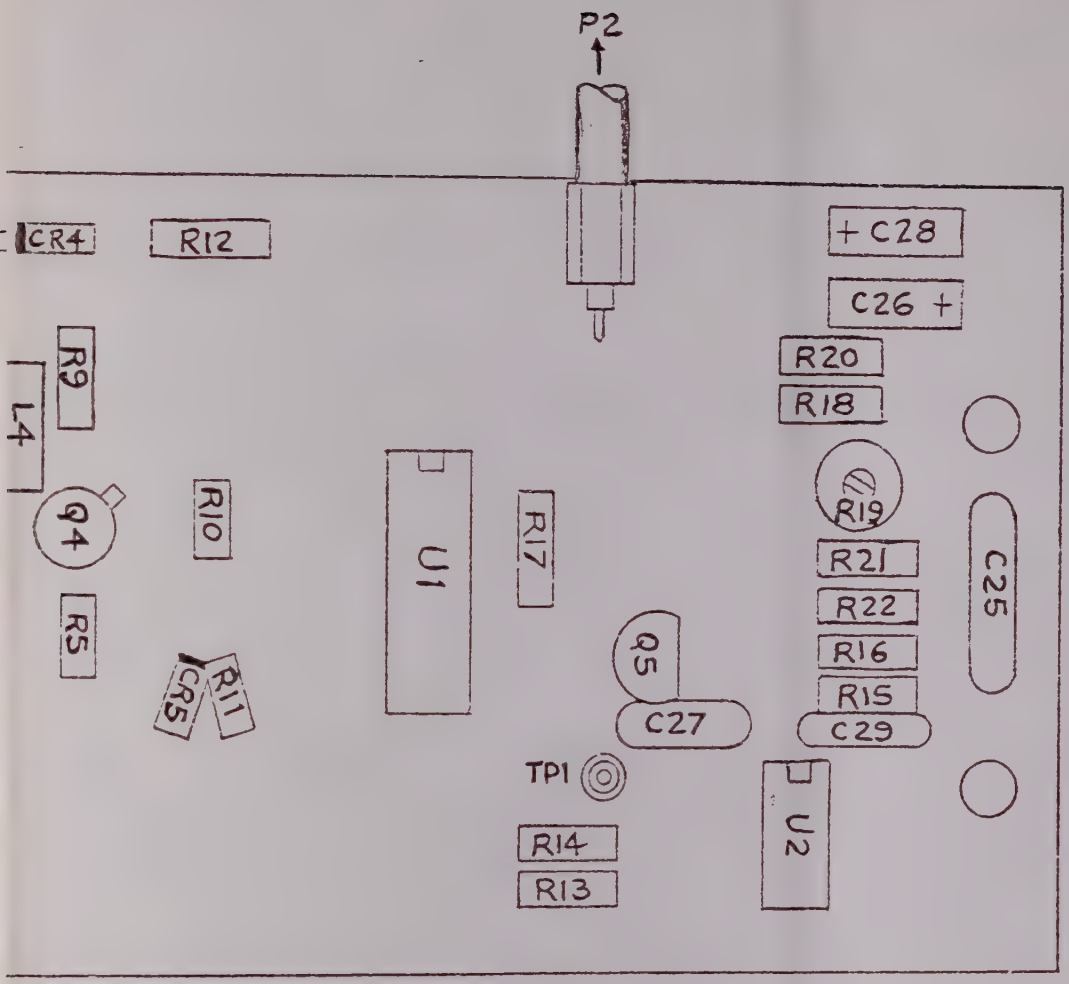
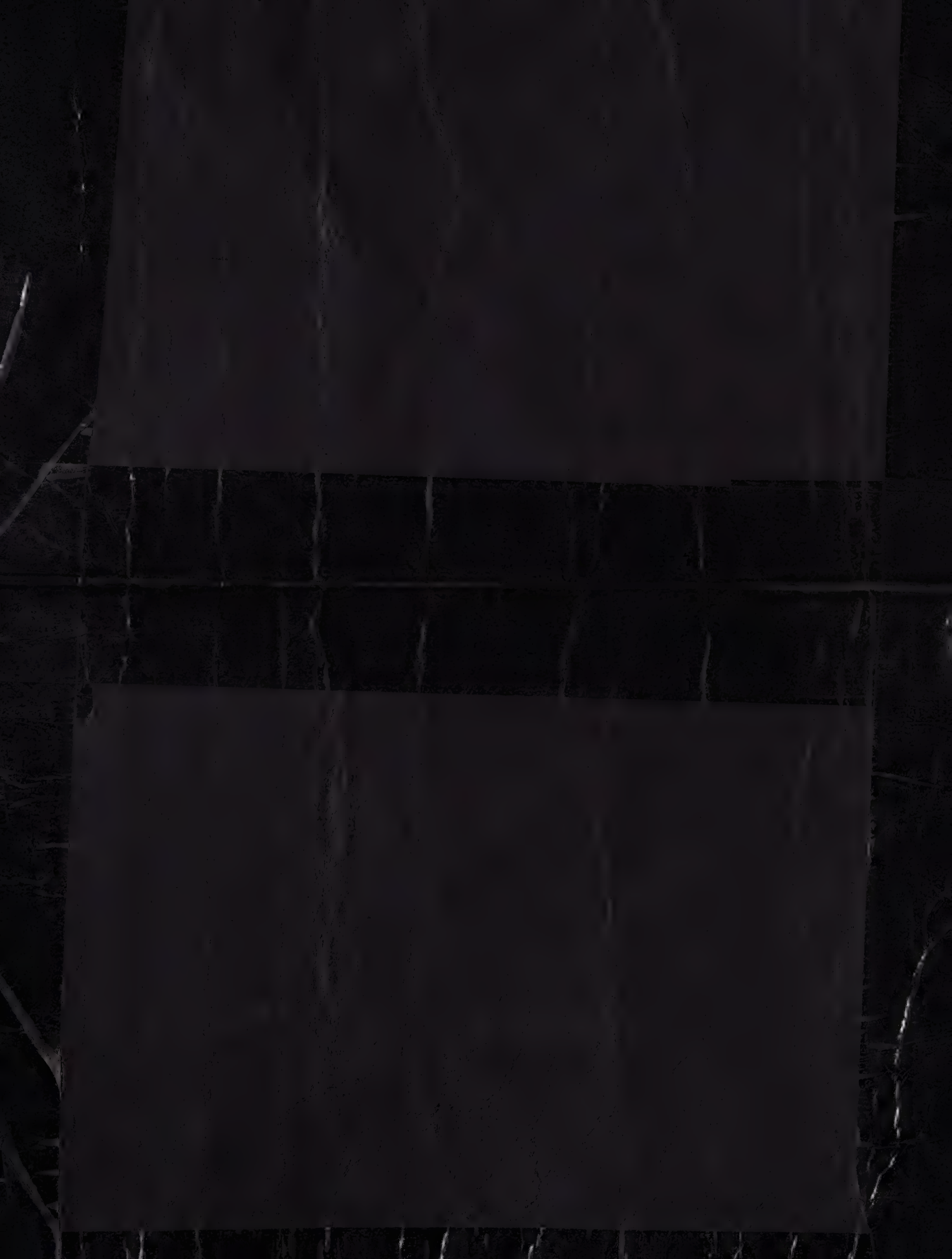
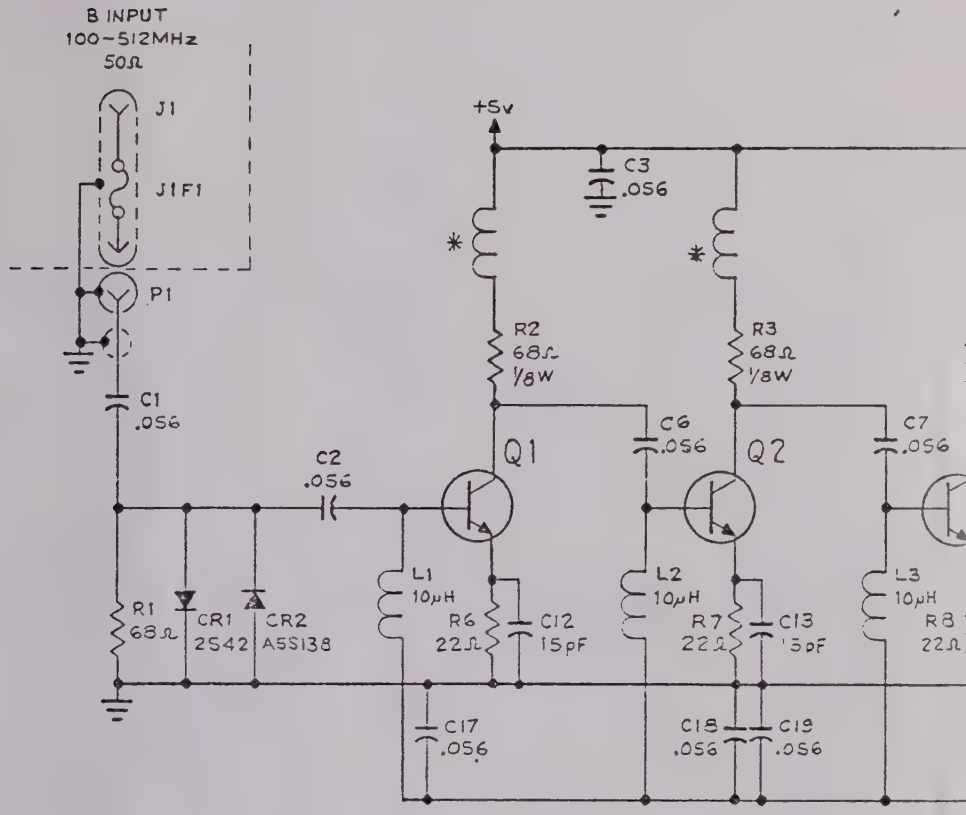
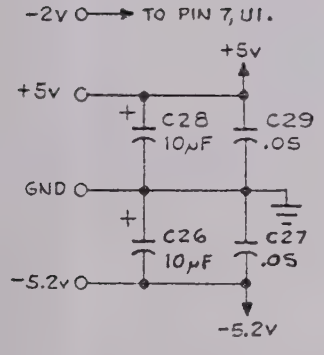


FIGURE 7-7
512 MHz PRESCALER (A1) ASSEMBLY
6042A #6729901 Rev B







	TYPE	+5v	-5.2v	-2v
U1	SP8613B	14		7
U2	SN72311P	8	1,4	

NOTE: (EXCEPT AS NOTED)

1) * — DENOTES PART OF PC PATTERN.

2) TRANSISTORS ARE 2N6304.

3) RESISTORS ARE 1/4W, 5%.
CAPACITORS ARE IN μF.

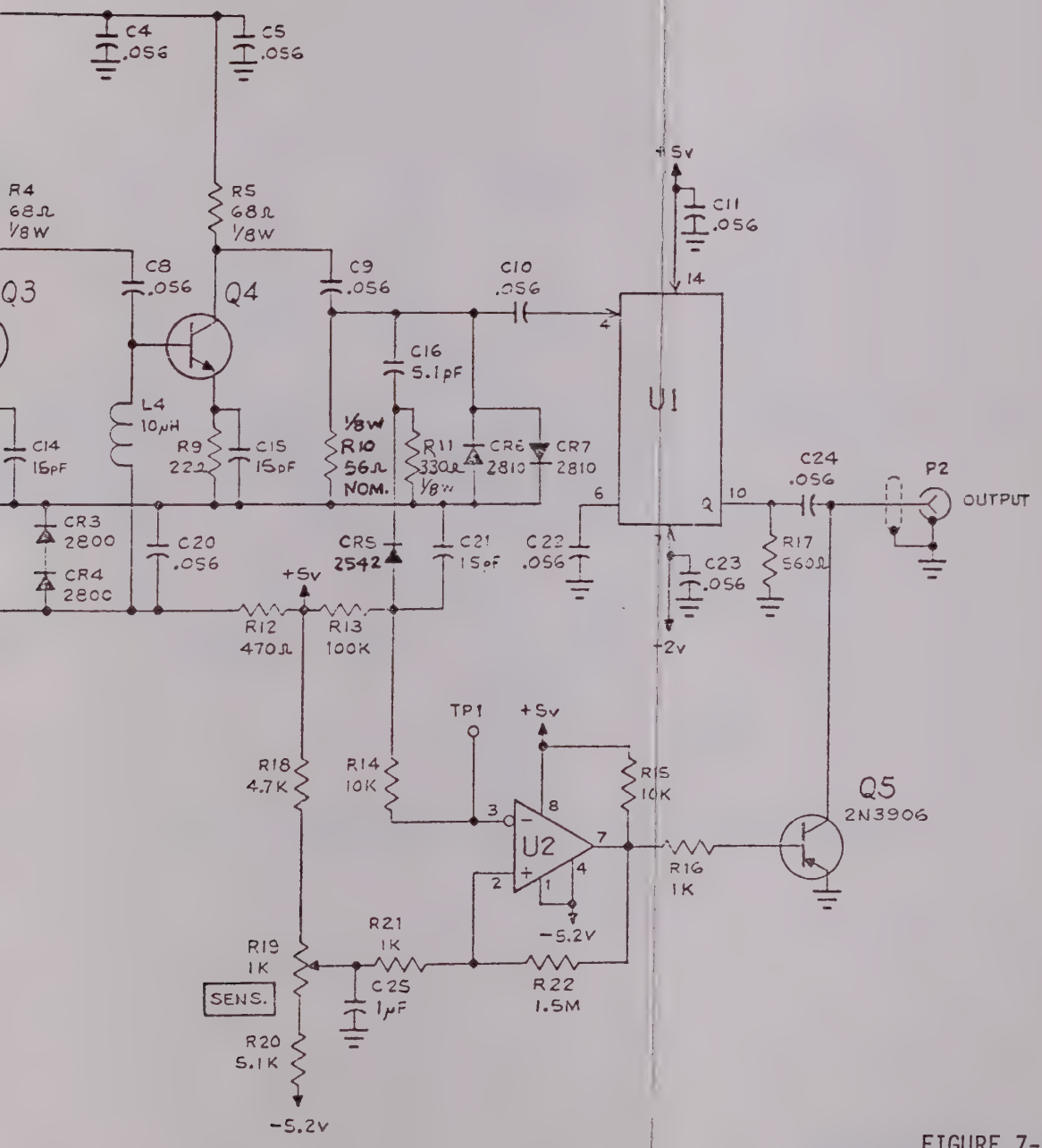
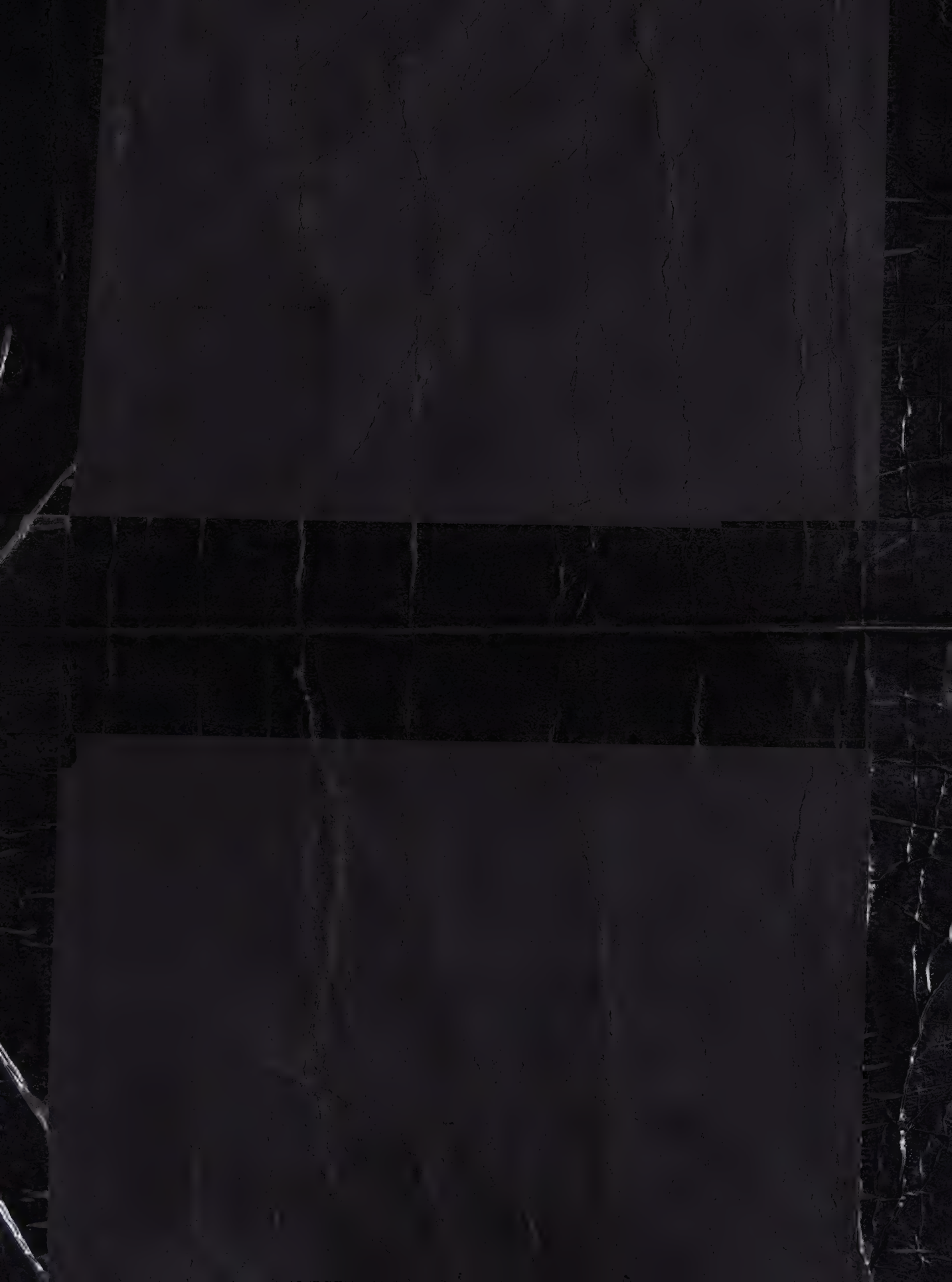
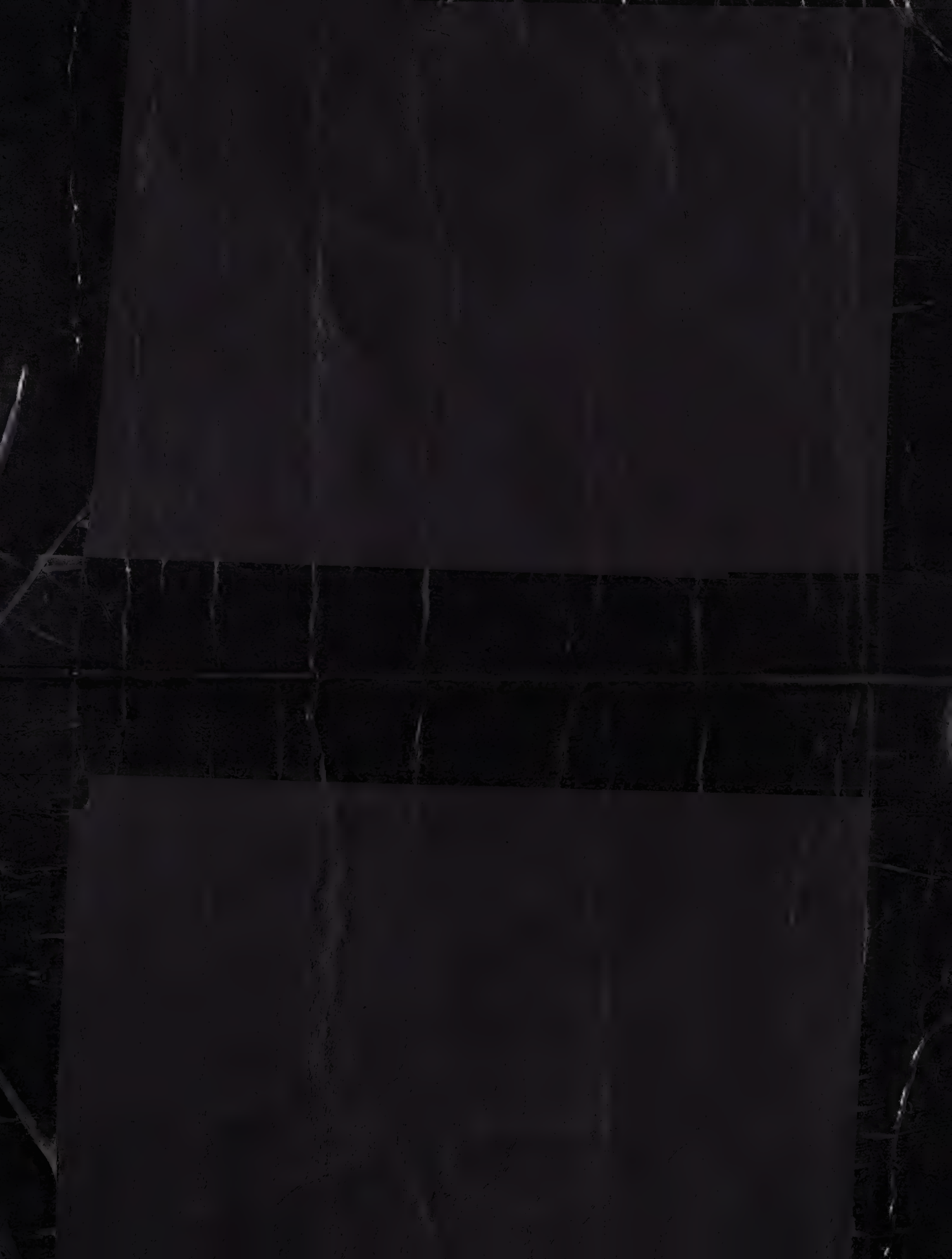


FIGURE 7-8
512 MHz PRESCALER (A1) SCHEMATIC
6042A #6729901 Rev A





C6
C8
C12
C13
L1
L2
L3
L4
P1
C1
C2
Q1
C4
Q2
C10
Q3
C15
Q4
CR1
CR2
R1
R3
R2
C11
R5
R4
R7
R6
C17
C18
C3
C7
C9
C5
C16
C14

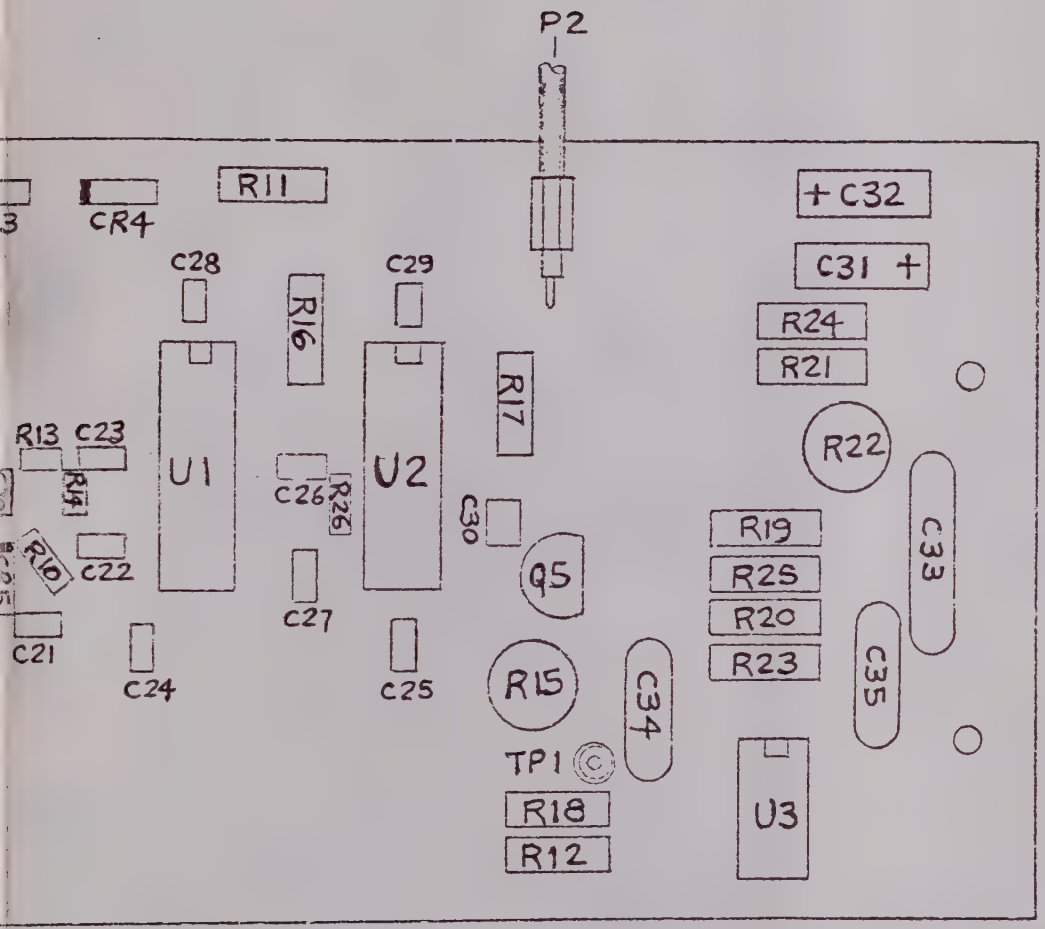
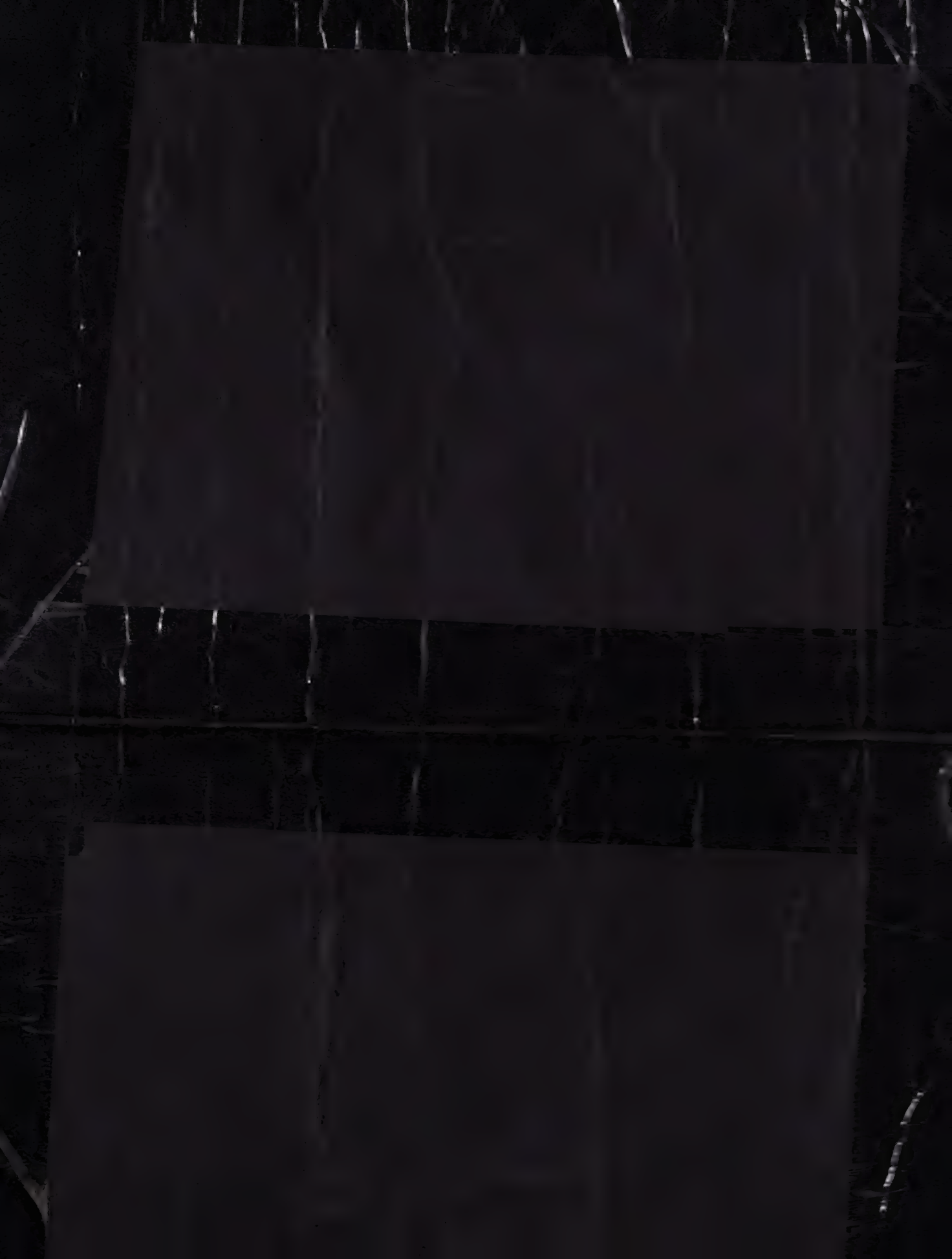
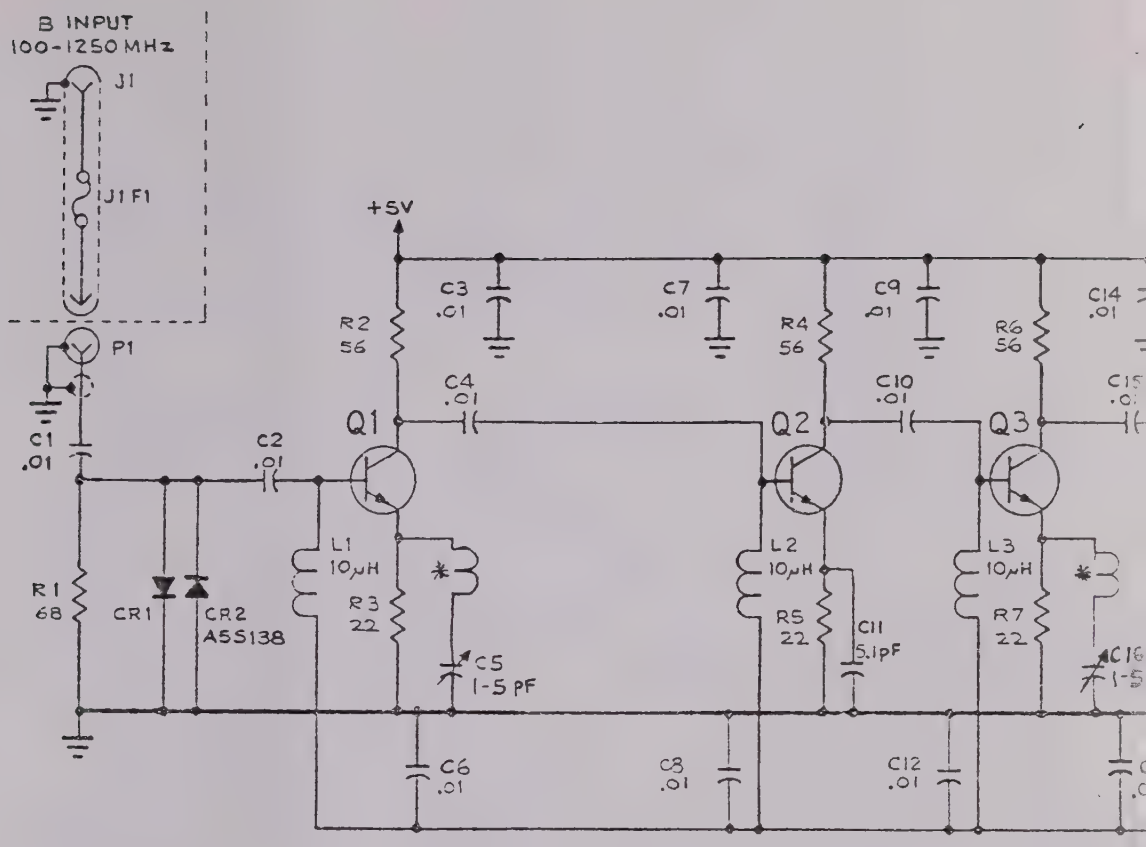


FIGURE 7-9
1.25 GHz PRESCALER (A1) ASSEMBLY
6043A #6725001 Rev B





TYPE		+5v	-5.2v	-2v
U1	SP8617B	14		—
U2	SP8617B	14		7
U3	SN723HP	8	1,4	

5. ALL DIODES ARE HPS082-2542.
4. ALL TRANSISTOR TYPES ARE BFR90
3. ALL CAPACITOR VALUES ARE IN μf
2. ALL RESISTOR VALUES ARE IN OHMS 5%, 1/4W
1. * P/O P.C. TRACE PATTERN

NOTE: UNLESS OTHERWISE SPECIFIED.

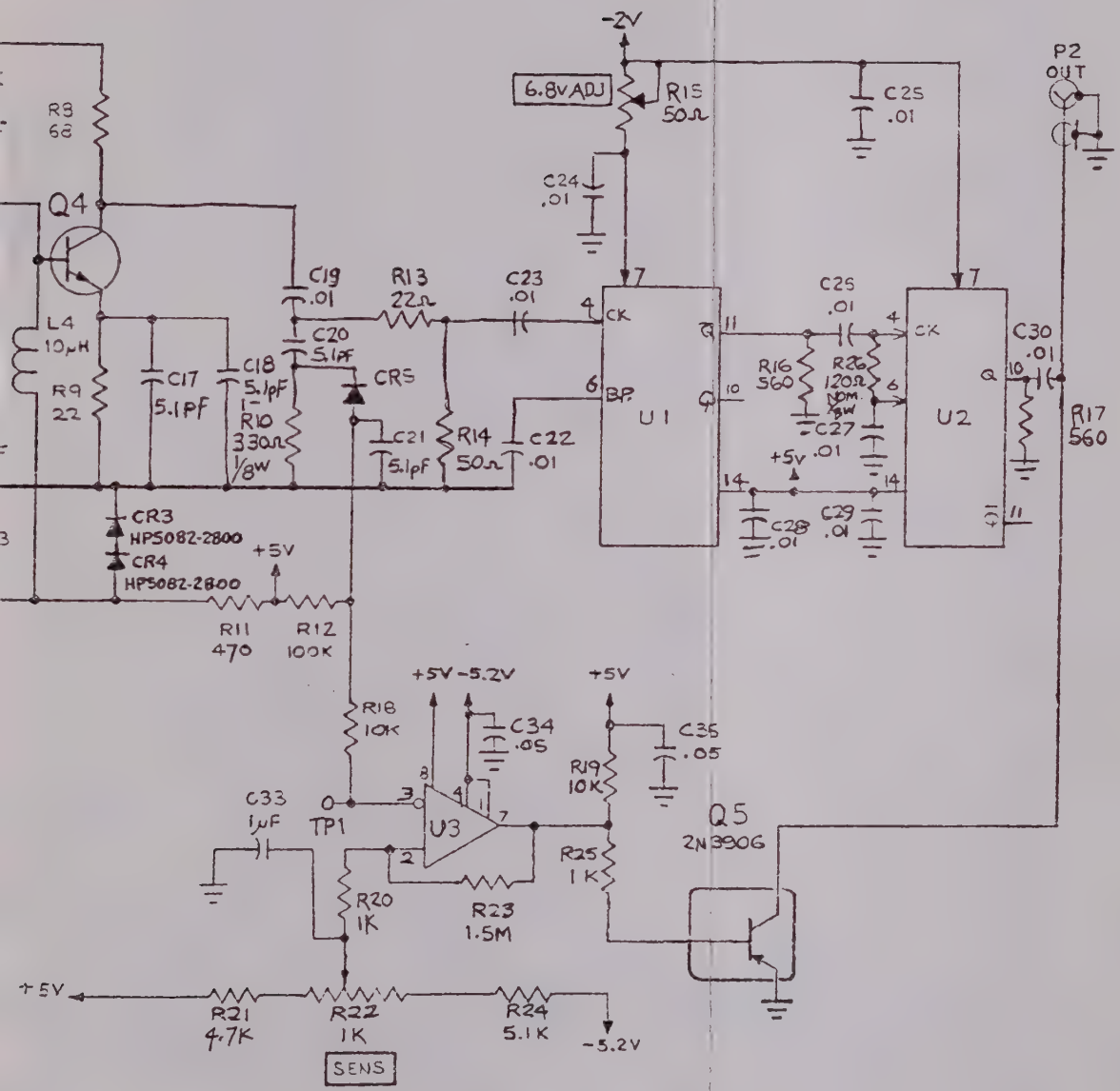
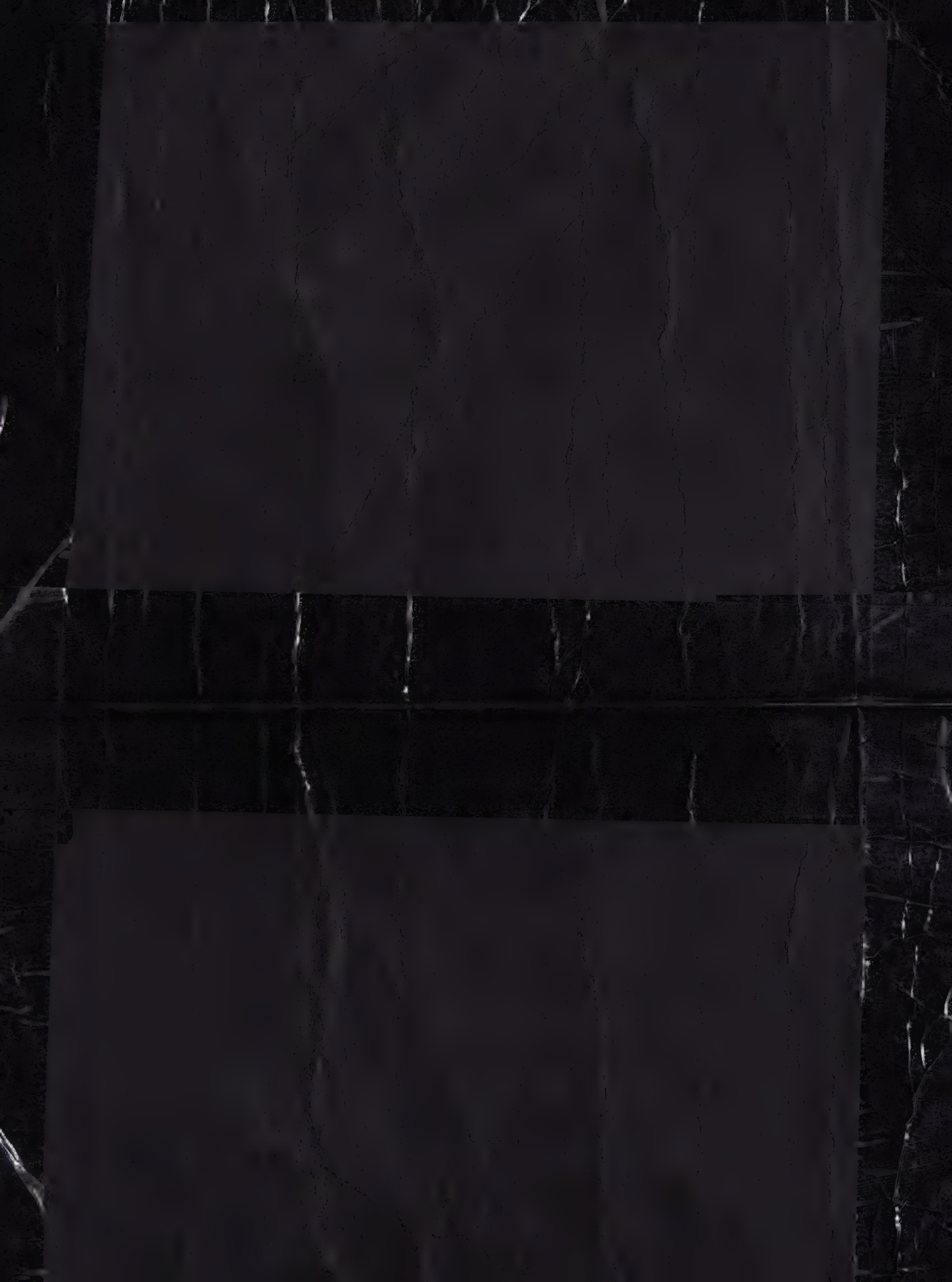
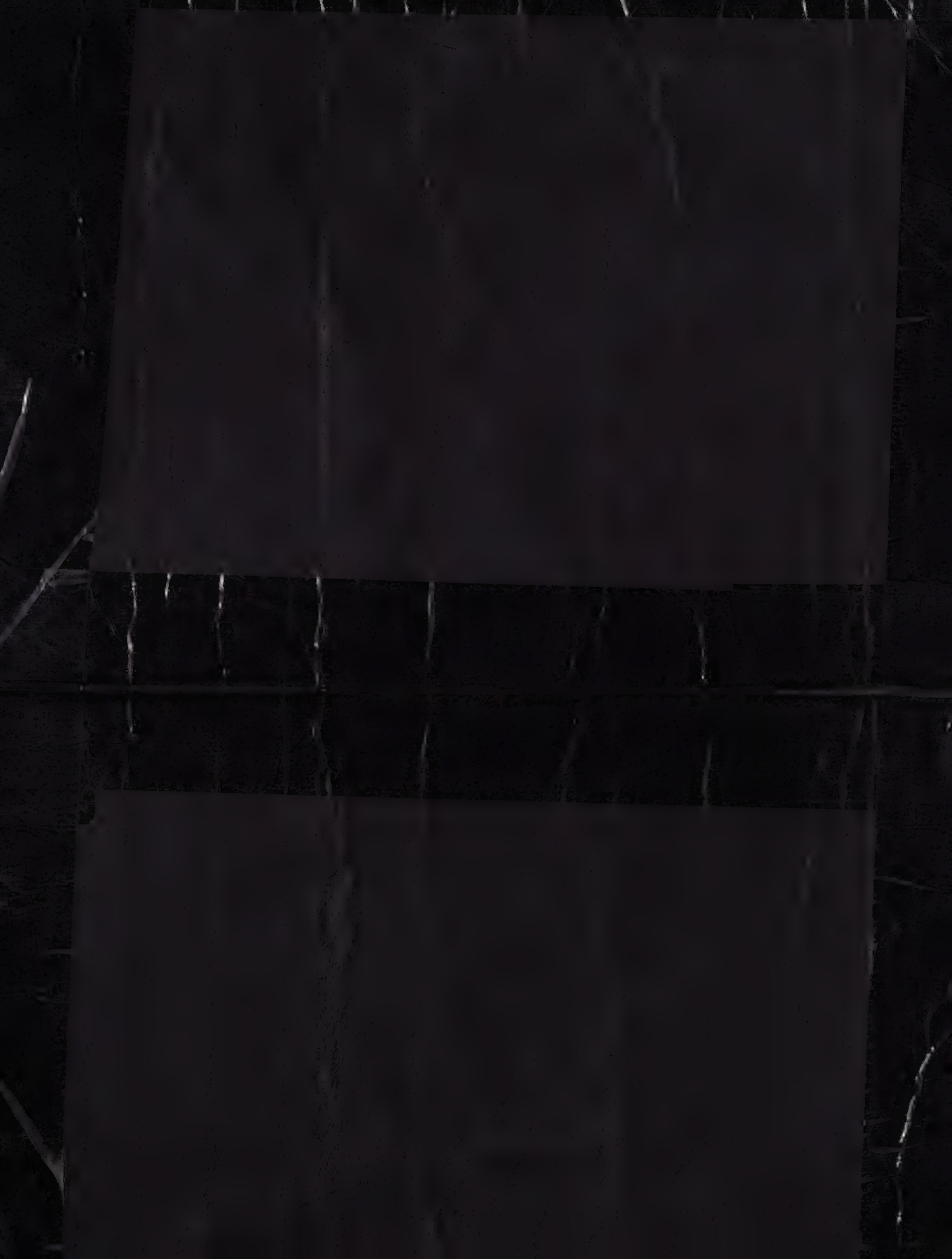


FIGURE 7-10
1.25 GHz PRESCALER (A1) SCHEMATIC
6043A #6725001 REV C





C17
U7
R30
R29
R32
R35
R34
R36
R33
R31
R37
R38
Q9
Q8
Q7
Q6
Q4
Q10
Q11
Q12
Q13
Q5
J3
R28
R44
R45
R51
U8
U9
U10
U6
U5
U4
U3
U2
U1
RN3
RN2
RN1
RN4
RN5
RN6
R52
C18
R24
R25
R23
R20
R19
J5
R27
C12
C13
R26
U12
U13
U14
J4
U17
S1
R58
U18
U19
U20
U23
U24
U25
U26
U27
U30
U32
U29
R16
R18
C8
C9
C34
C33
C38
CR2
CR3
C2
R1
R5
R12
R13
C29
C11
R17
R14
C20
R54
R57
R15
C35
R59
R6
R10
R8
R9
R7
C10
C37
R11
R4
C7
C6
Q1
Q2
CR1
R3
XK1
K1
R60
C5
R21
R22
C4
R2
C3
C1
Q3
R55
CR8

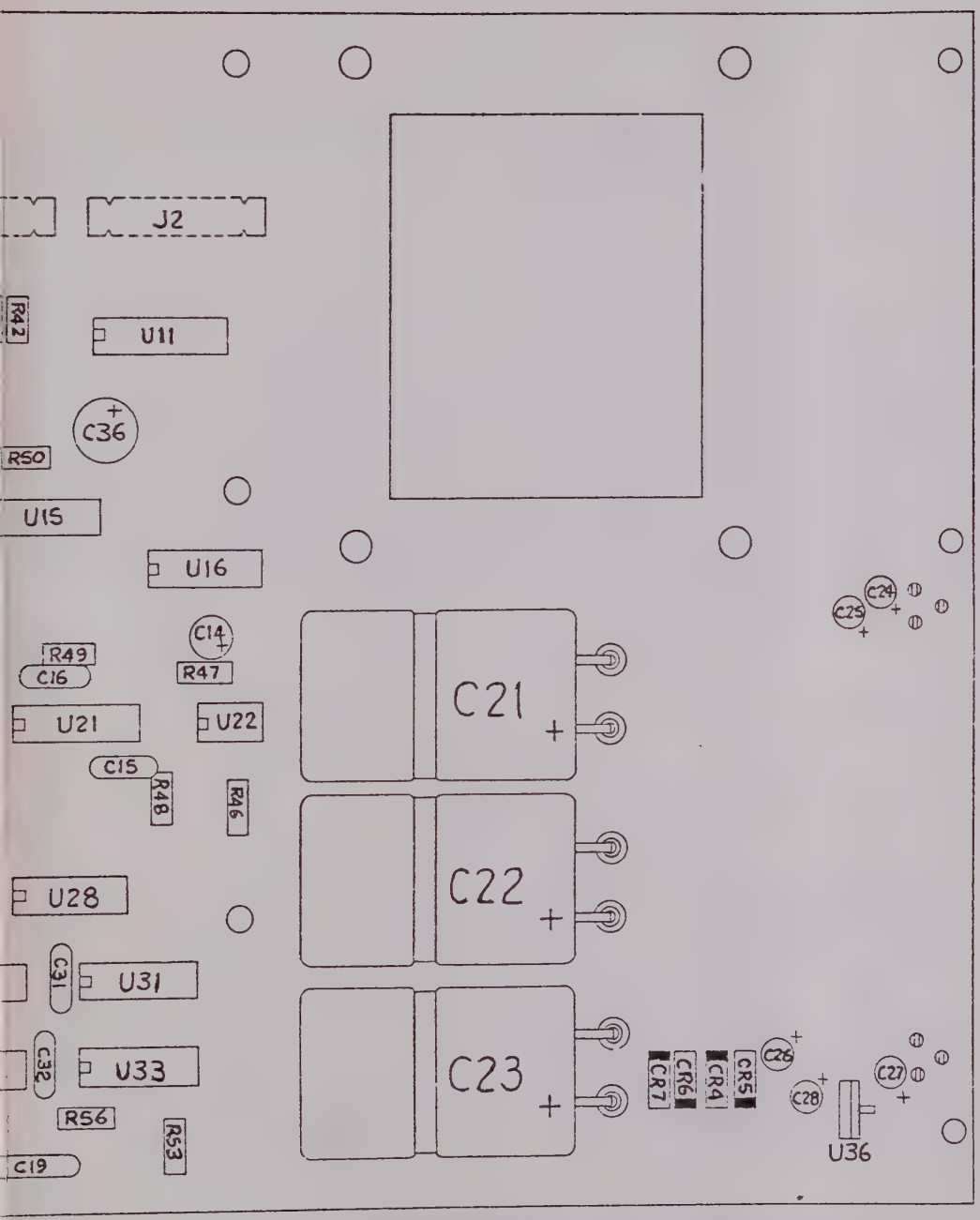
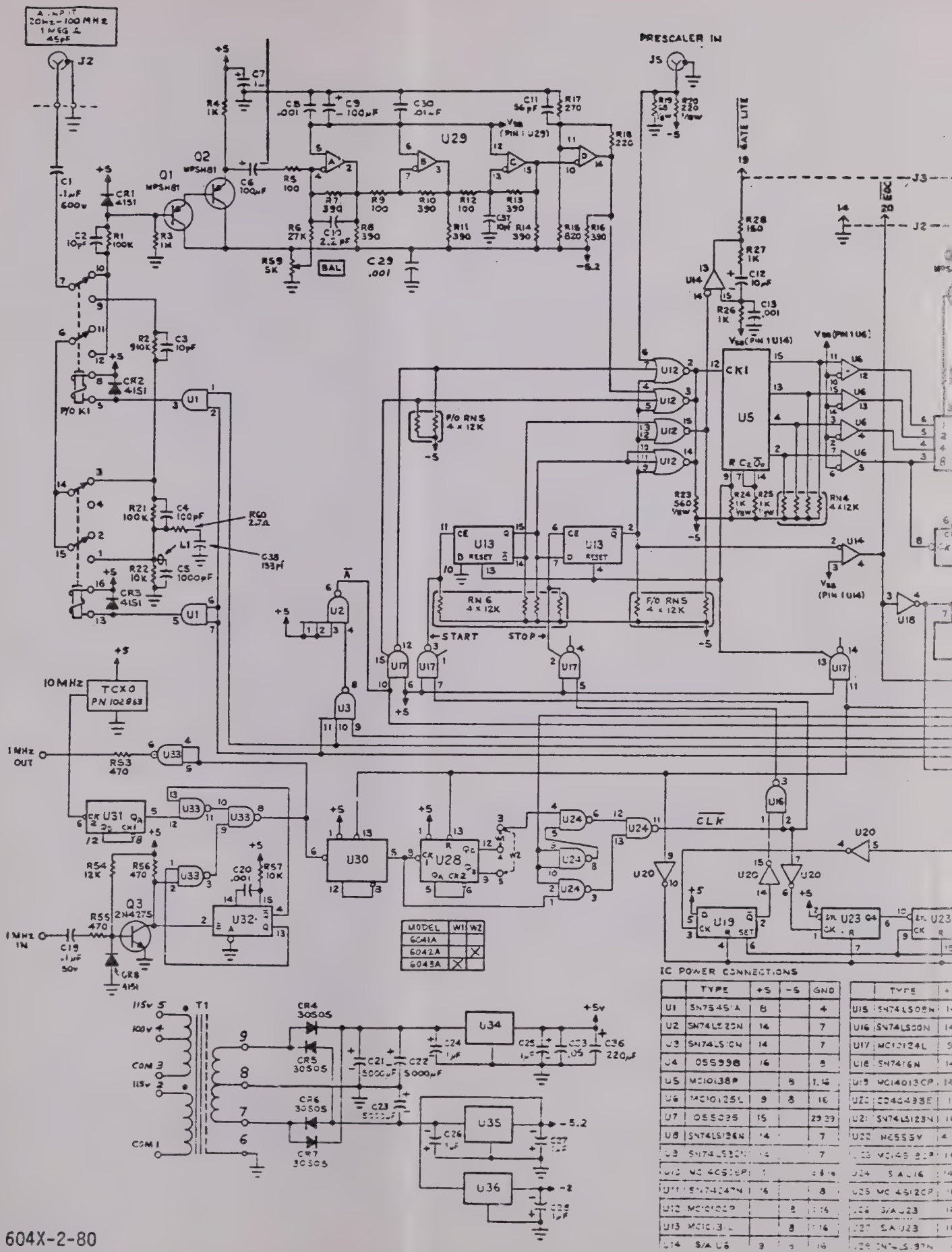
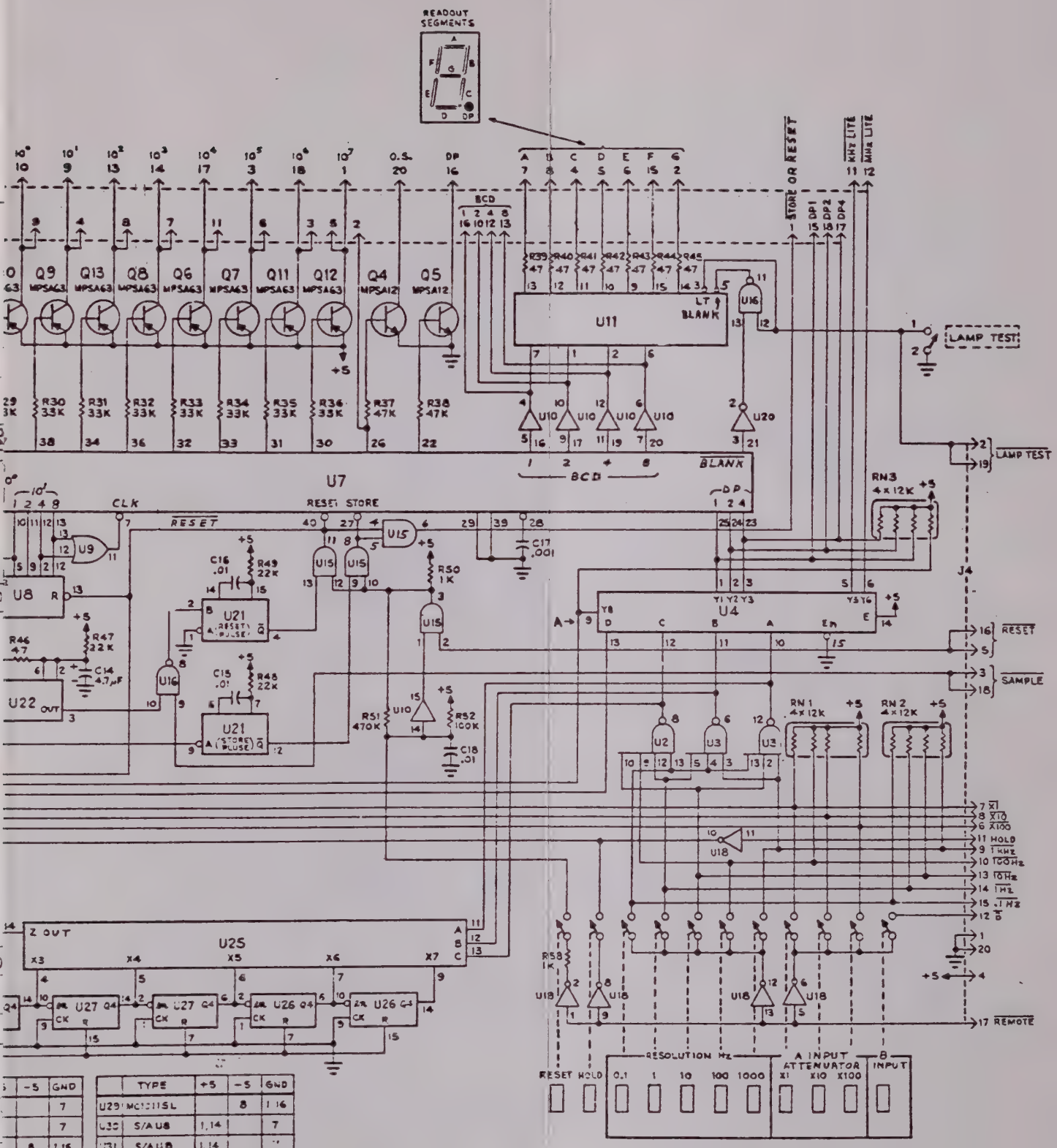


FIGURE 7-11
LOGIC (A2) ASSEMBLY
#6725201 Rev B



	TYPE	+5	-5	GND
U1	SN7545*A	8		4
U2	SN74LS20N	14		7
U3	SN74LS10N	14		7
U4	055998	16		8
U5	MC10138P		5	1,16
U6	MC10125L	9	8	16
U7	055035	15		29,39
U8	SN74LS136N	14		7
U9	SN74LS30N	14		7
U10	MC 4053BCP	1		8,16
U11	SN74247N	16		8
U12	MC10102P		8	16
U13	MC10131L		8	16
U14	S/A U6	8	5	16

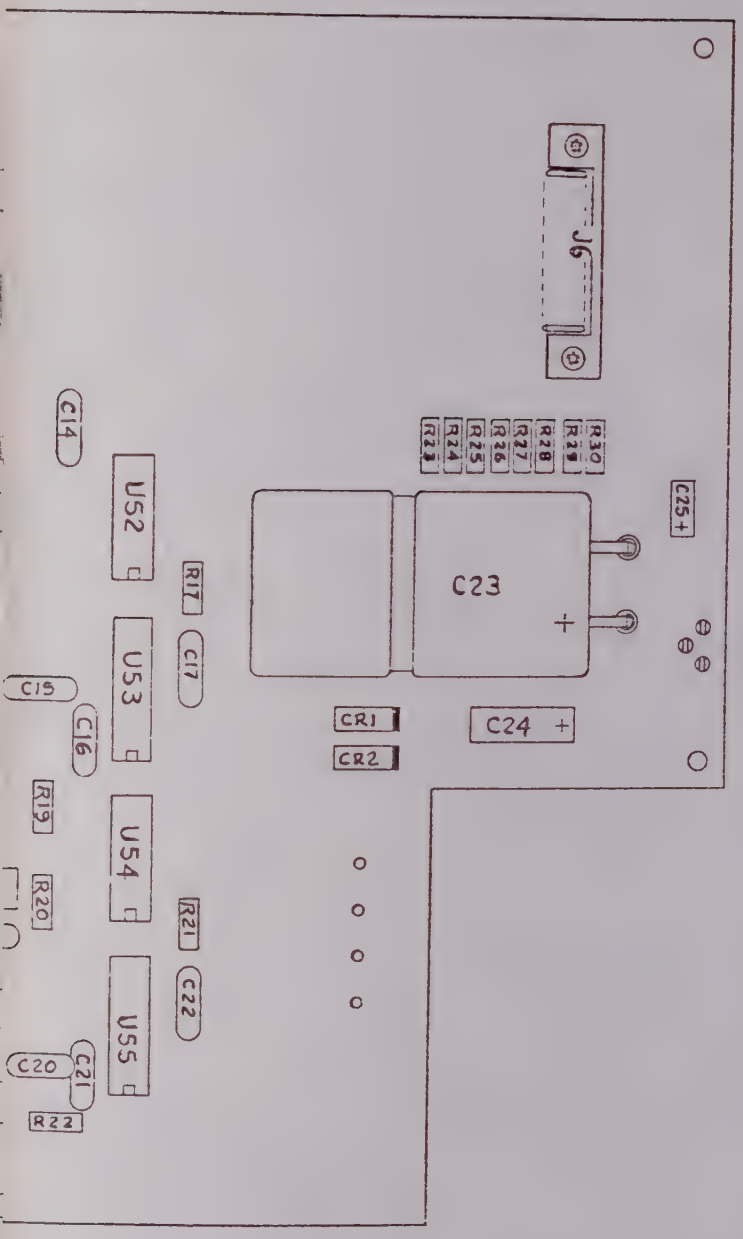
	TYPE	+
U15	SN74LS08N	14
U16	SN74LS00N	14
U17	MC10124L	5
U18	SN7416N	14
U19	MC14013CP	14
U20	CD4049BE	16
U21	SN74LS123N	16
U22	NE555V	4
U23	MC14538BCP	16
U24	S/A U16	14
U25	MC 4512CP	16
U26	S/A U23	16
U27	S/A U23	16
U28	SN74LS37N	14

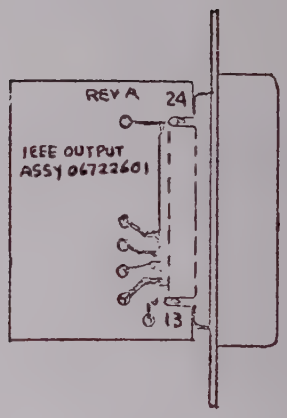


	TYPE	+5	-5	GND
U29	MC1011SL		8	1 16
U30	S/A U8	1,14		7
U31	S/A U8	1,14		7
U32	S/A U21	16		1,8
U33	S/A U16	14		7
U34	MC7805CP	—	—	—
U35	MC7905.2CP	—	—	—
U36	MC7902CT	—	—	—

FIGURE 7-12
LOGIC (A2) SCHEMATIC
#6725201 Rev B

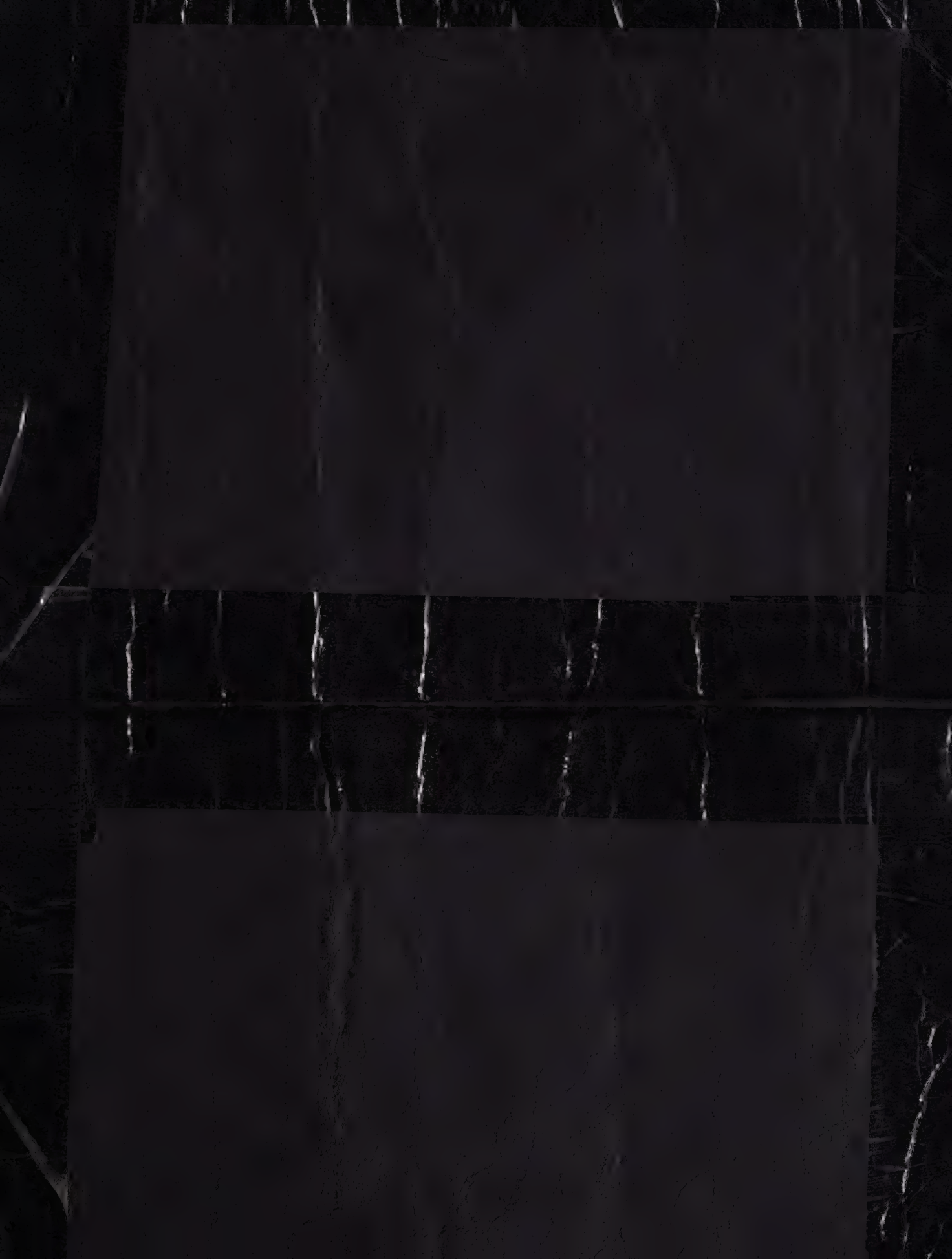
S1
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
U30
U31
U32
U33
U34
U35
U36
U37
U38
U39
U40
U41
U42
U43
U44
U45
U46
U47
U48
U49
U50
U51
J2
J3
J4
RN1
RN2
RN3
RN4
RN5
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R18
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C18
C19
C26
Q1

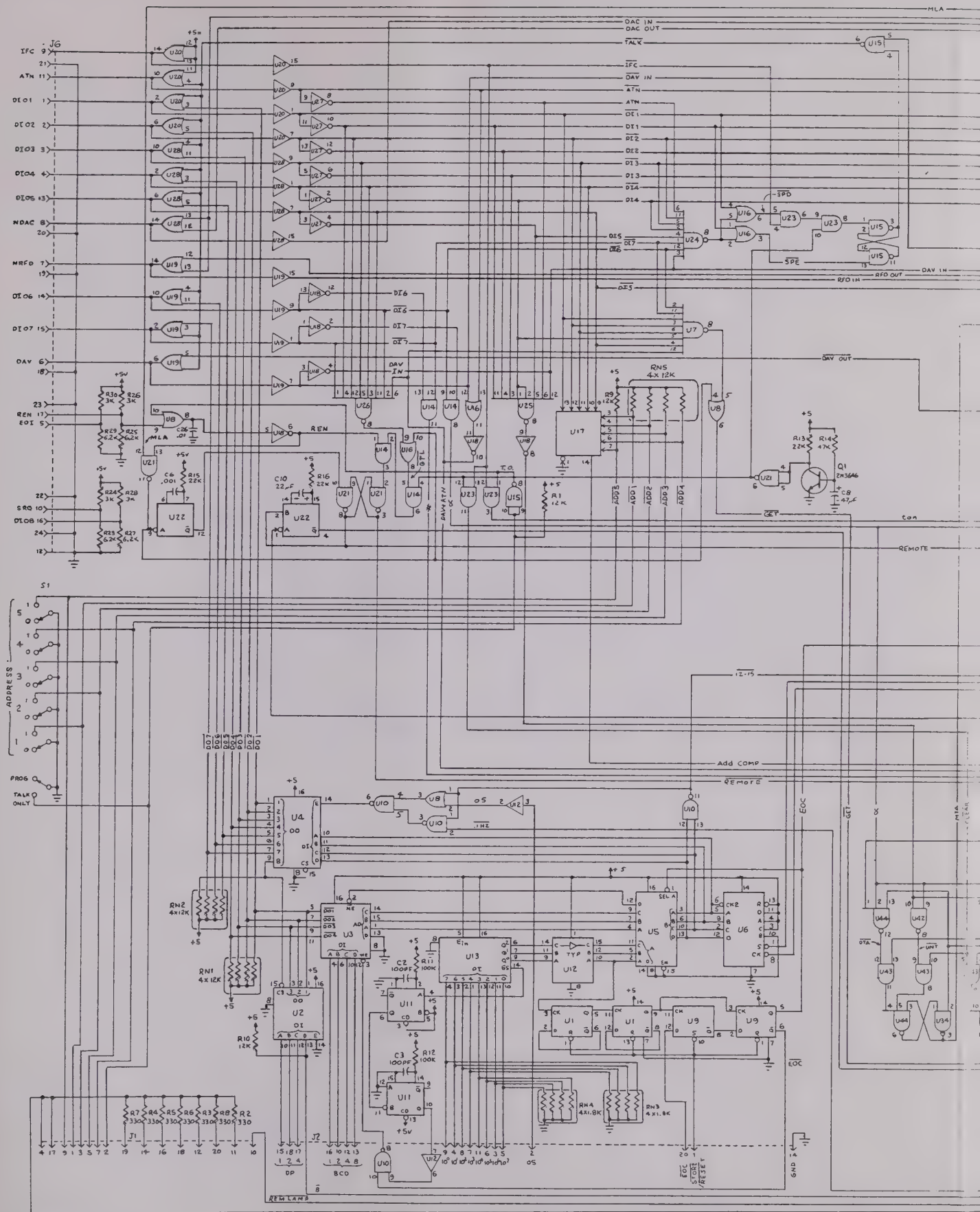




IEEE OUTPUT PC ASSEMBLY A5
(P/N 06722601)

FIGURE 7-13
IEEE-488 INTERFACE (A3) ASSEMBLY
#6720301 Rev A




MLA
DAC IN
DAC OUT
TALK
IFC
DAV IN
ATN
DI1
DI2
DI3
DI4
DI5
DI6
DI7
SPD
SPE
RFD IN
RFD OUT
DAV OUT
REN
EOI
SRQ
DIO8
NDAC
NRFD
DAV
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
J6
RN5
4-X 12K
REMOTE
ADDRESS
PROG
TALK ONLY
S1
Add COMP
REMOTE
EOC
GET
MTA
RN1
4X 12K
RN2
4X12K
RN3
4X1.8K
RN4
4X1.8K
J1
J2
DP
BCD
REMLAB
GND
STORE
RESET

604X-2-80

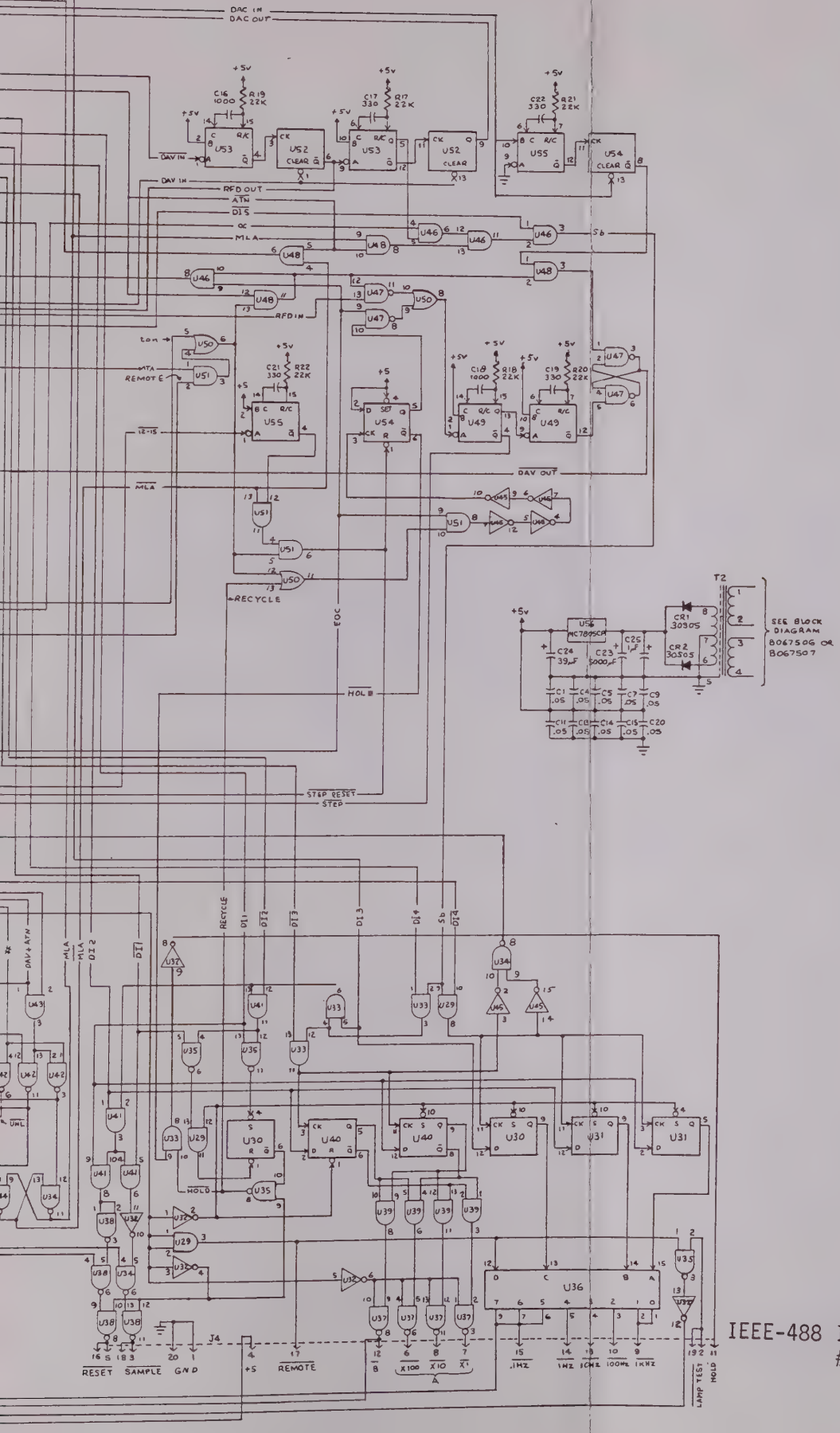
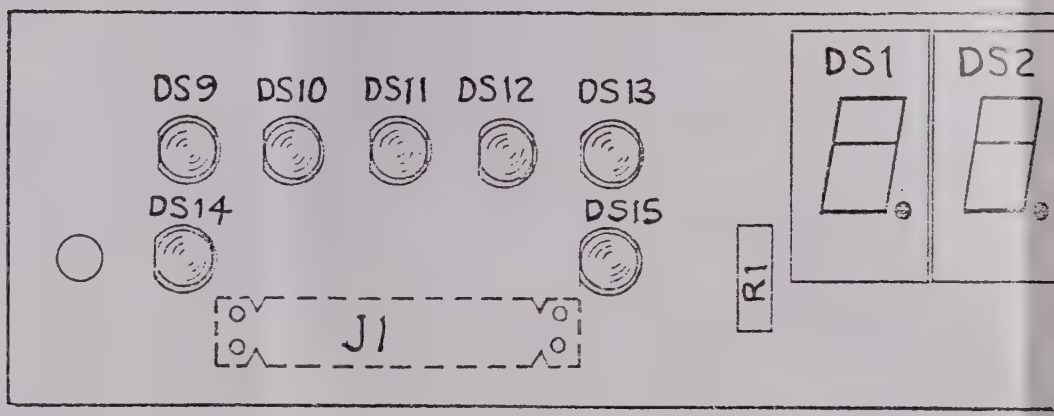


FIGURE 7-14
IEEE-488 INTERFACE (A3) SCHEMATIC
#6720301 Rev A


DS9
DS10
DS11
DS12
DS13
DS14
DS15
J1
R1
DS1
DS2

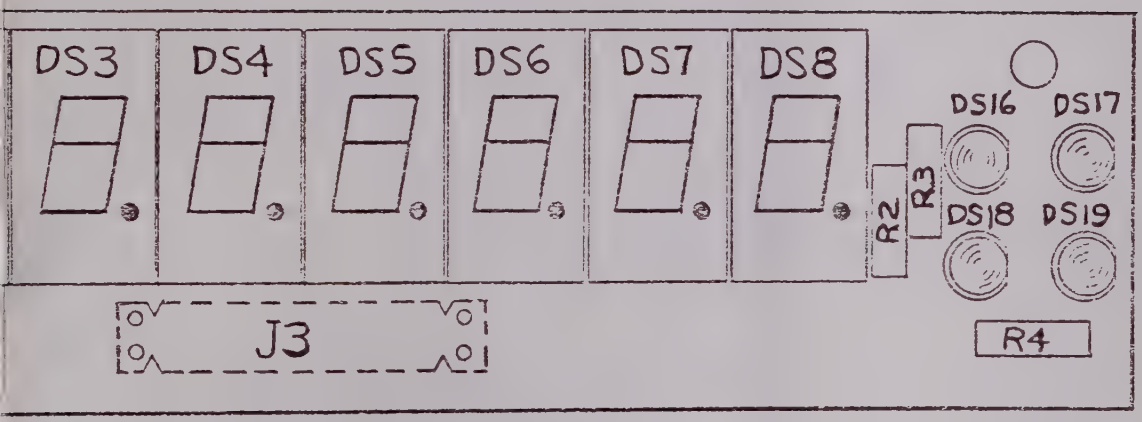
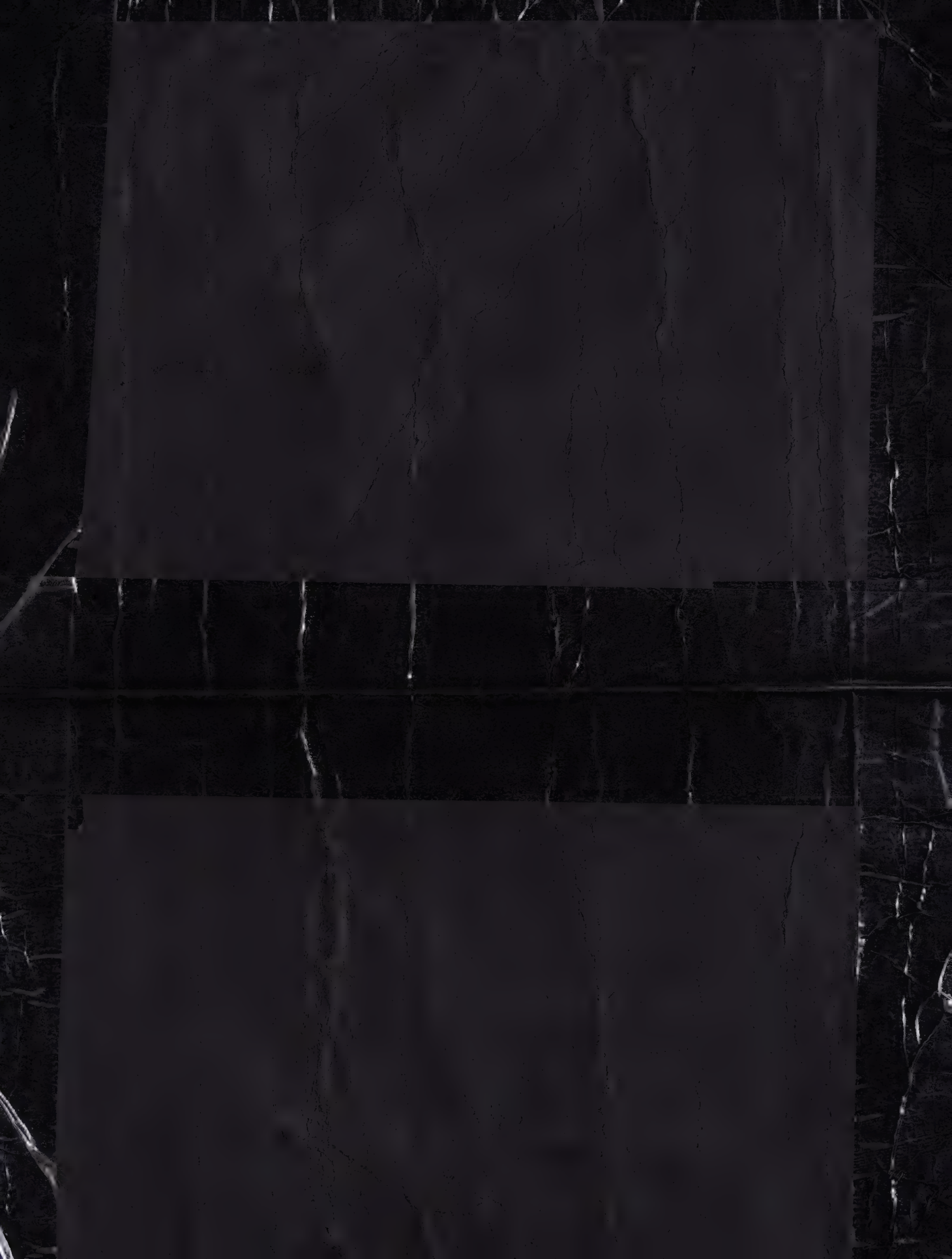
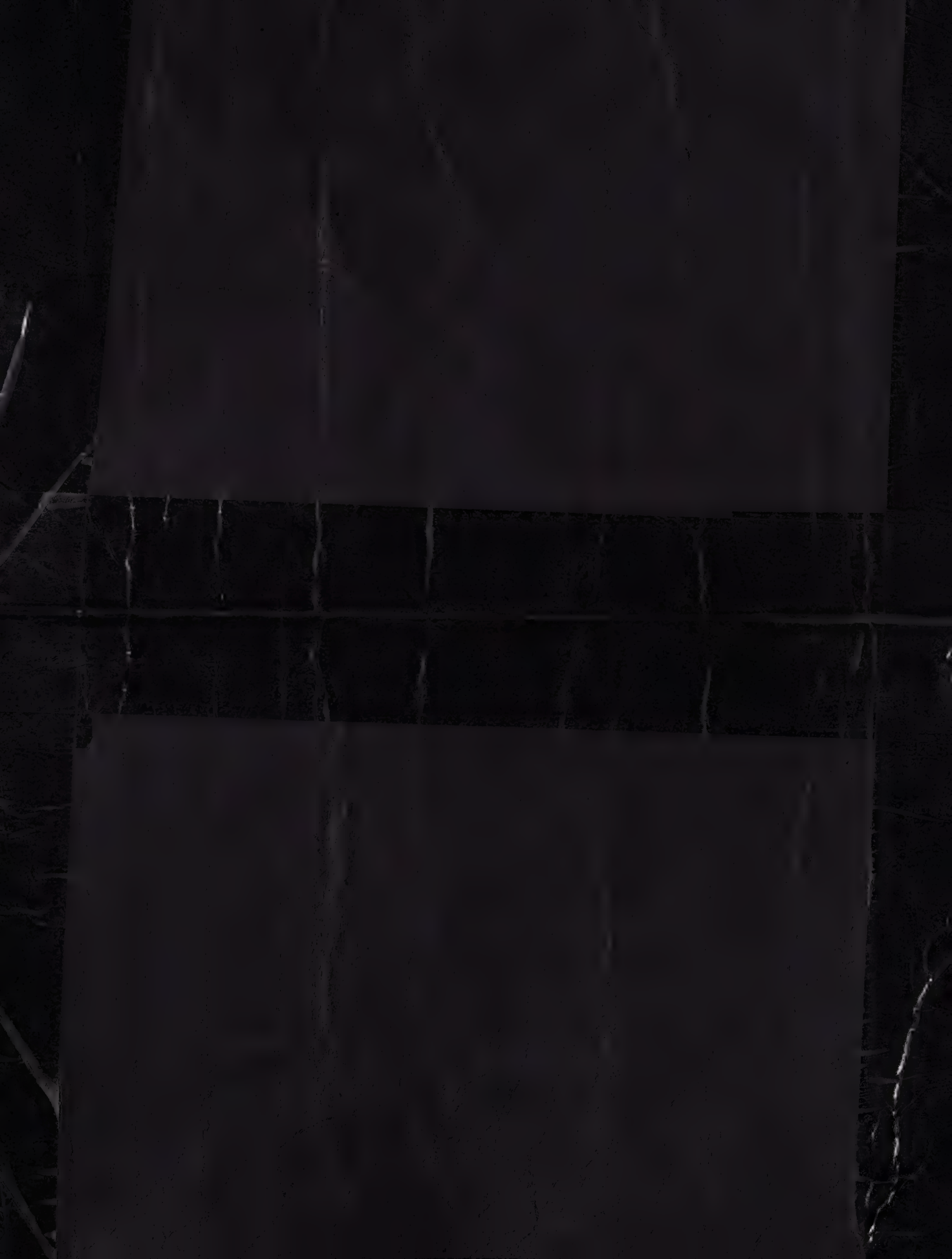
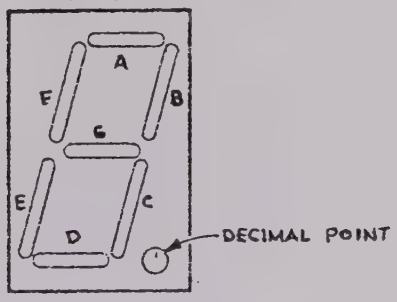


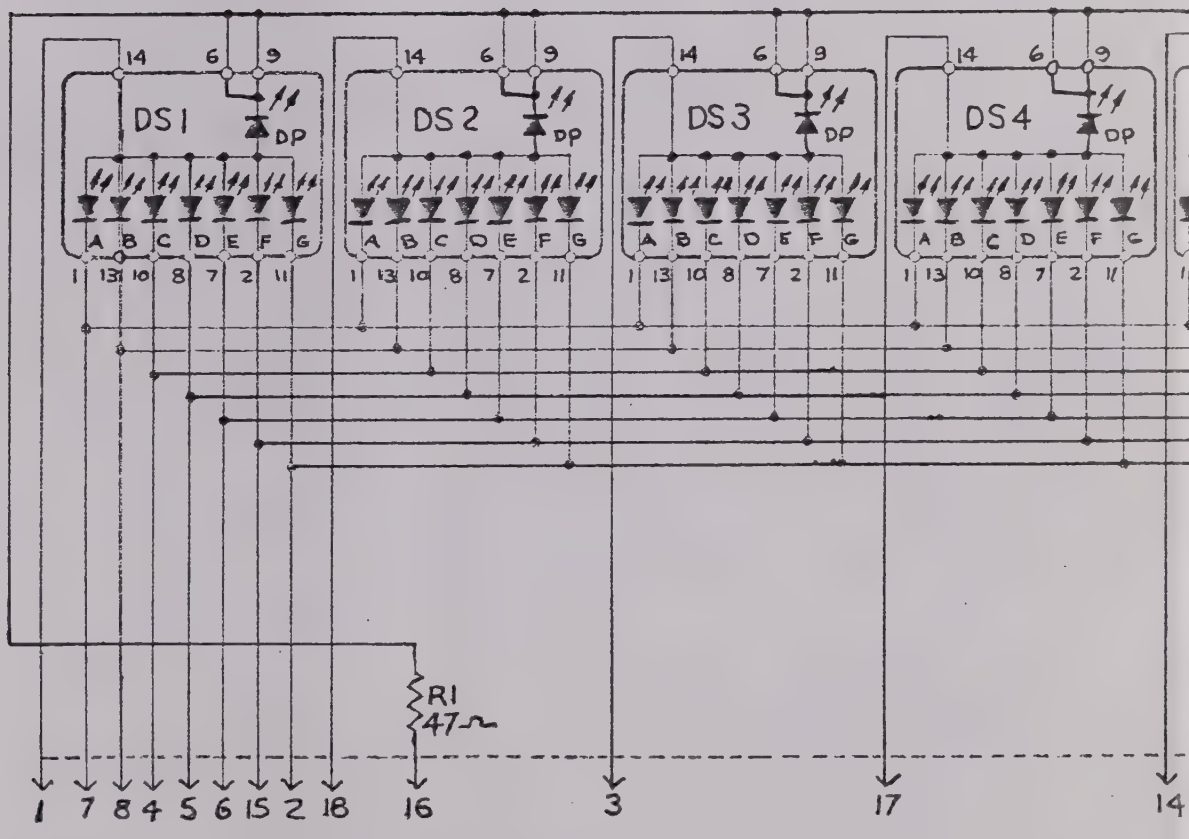
FIGURE 7-15
DISPLAY (A4) ASSEMBLY
#6722901 Rev A





DS1 THRU DS8 ARE
SEVEN SEGMENT
LED DISPLAYS
MAN 3610





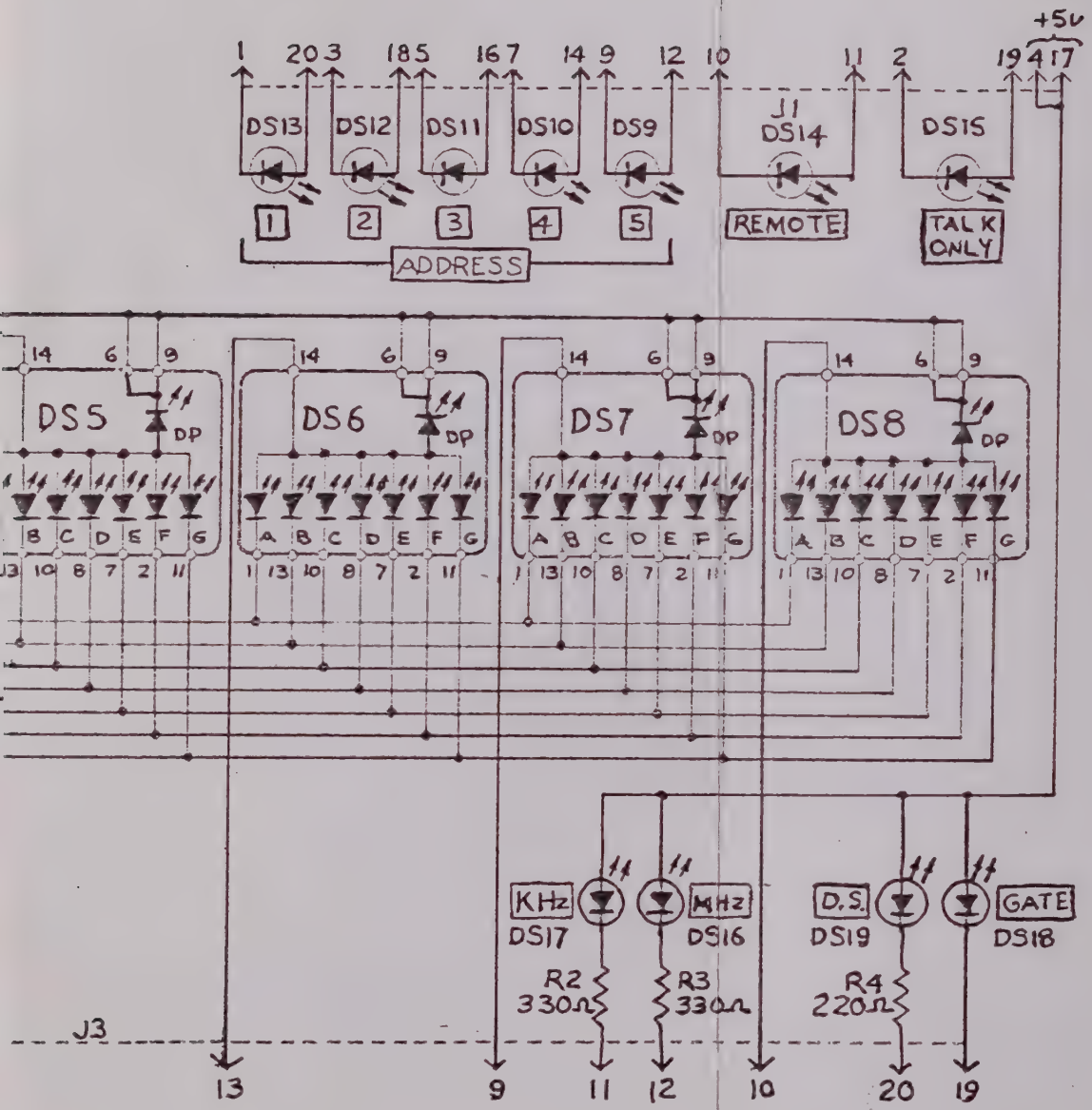


FIGURE 7-16
DISPLAY (A4) SCHEMATIC
#6722901 Rev A

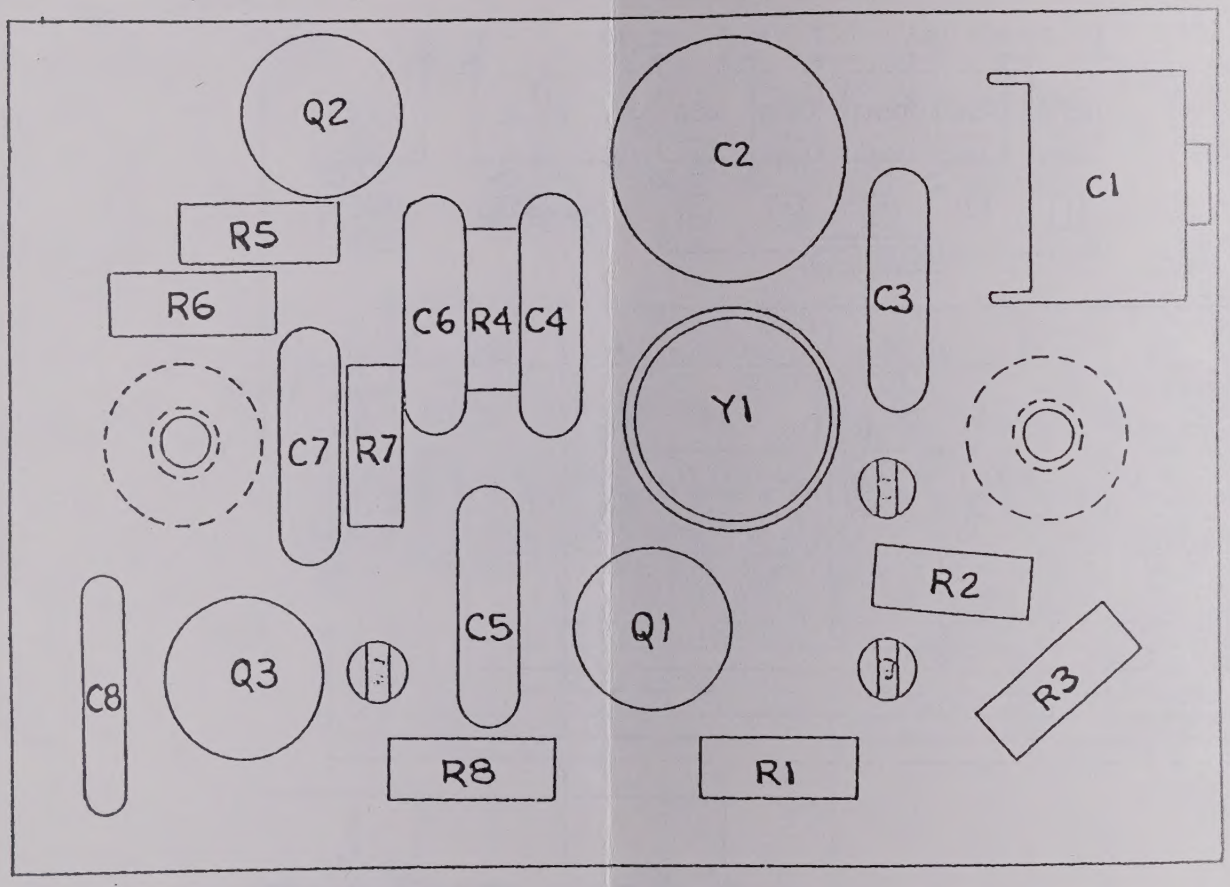


FIGURE 7-17
OSCILLATOR ASSEMBLY
#5746802 Rev A

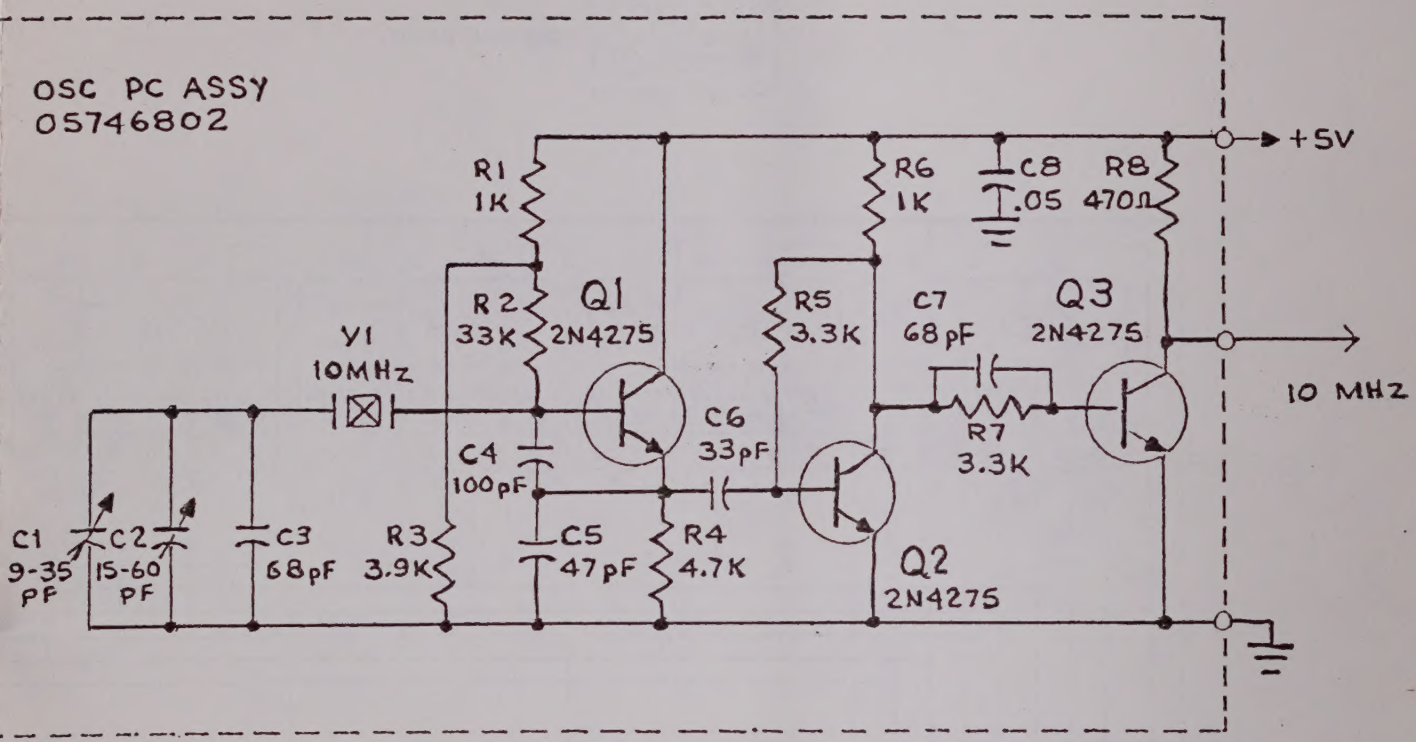


FIGURE 7-18
OSCILLATOR SCHEMATIC
#5746802 Rev A

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